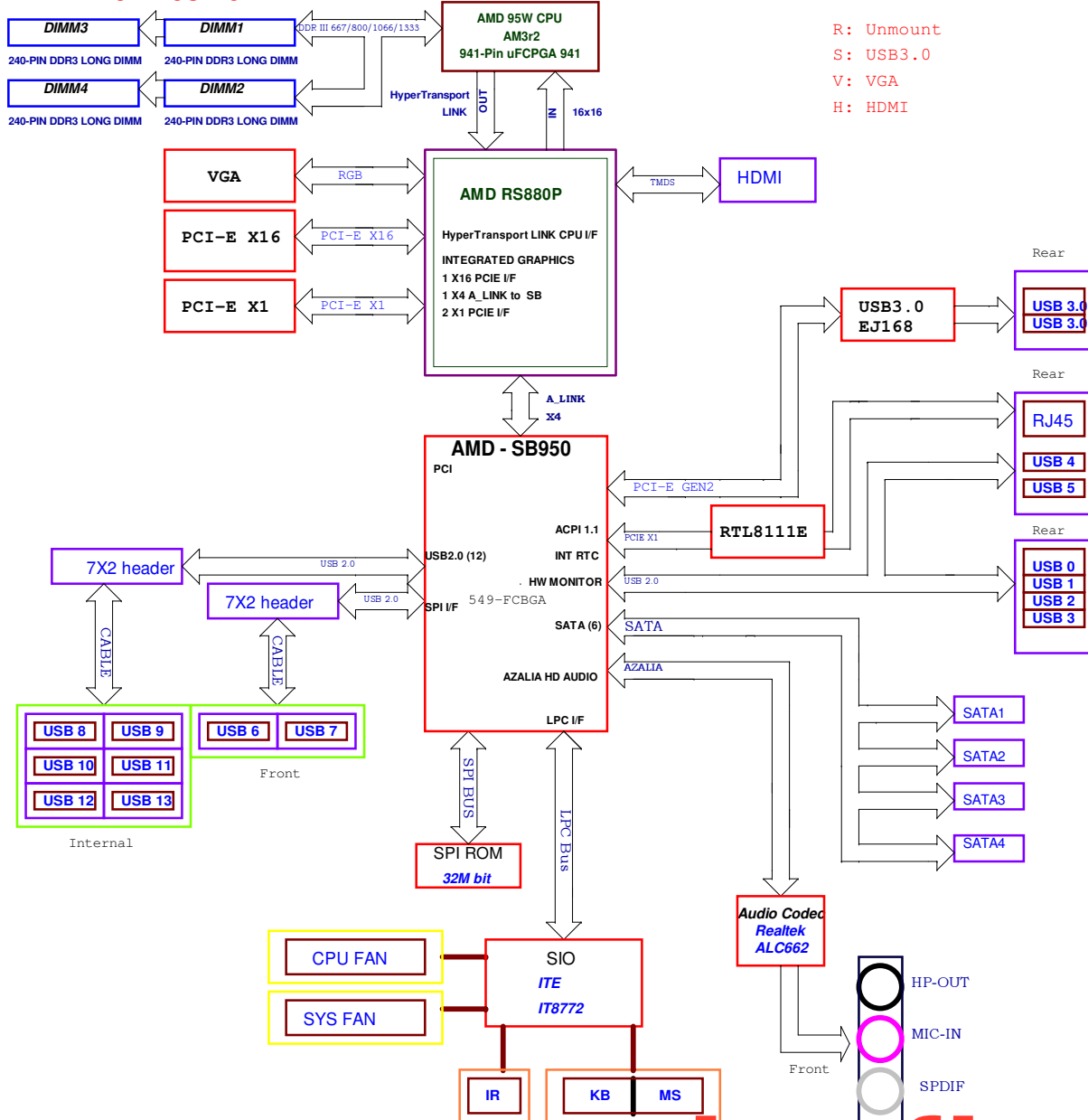


PROJECT NAME:NADIA
BOARD VERSION:10108-1
DATE: 2011.03.10

AMD RS880P+SB950 **Block Diagram**

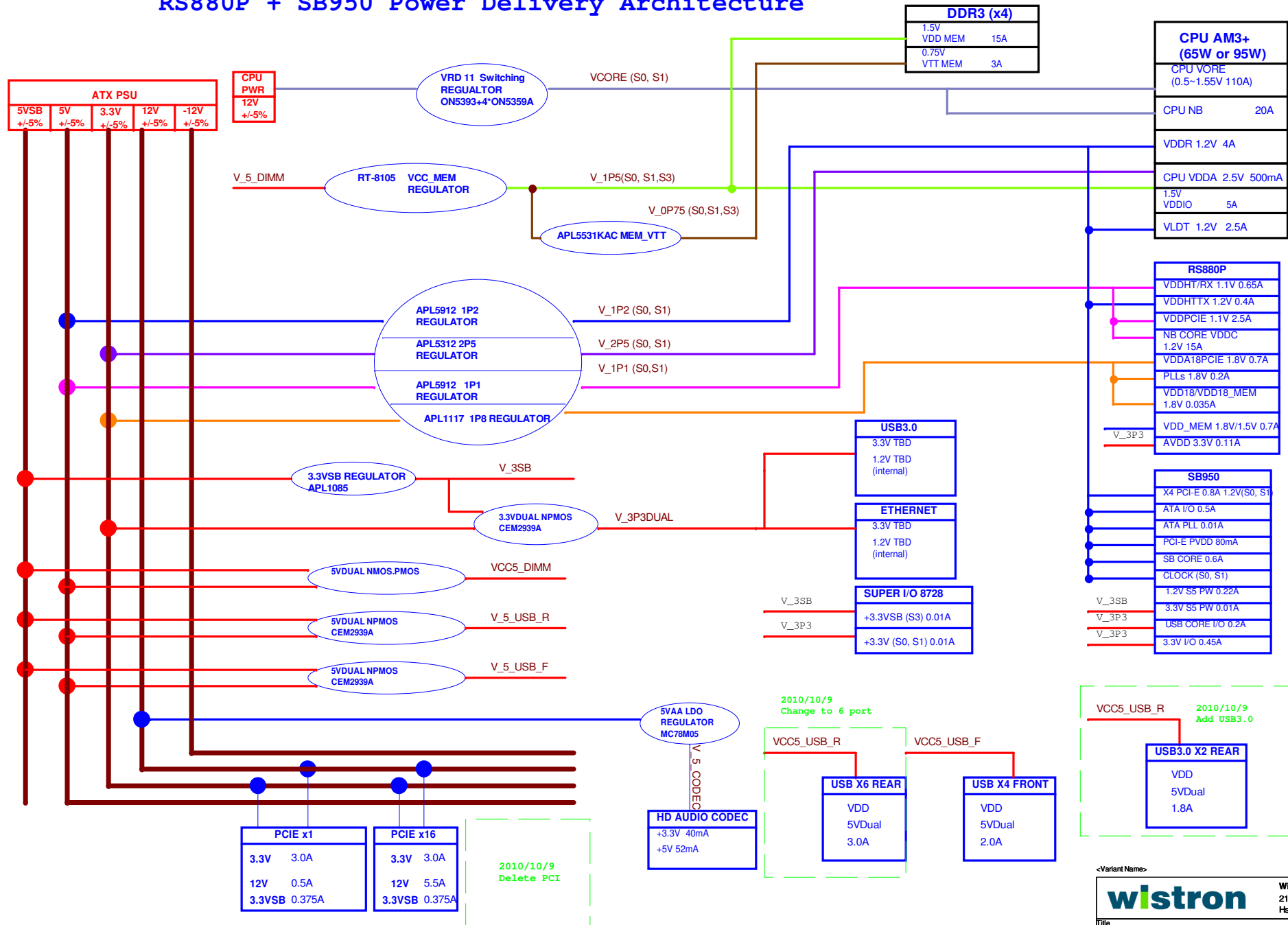
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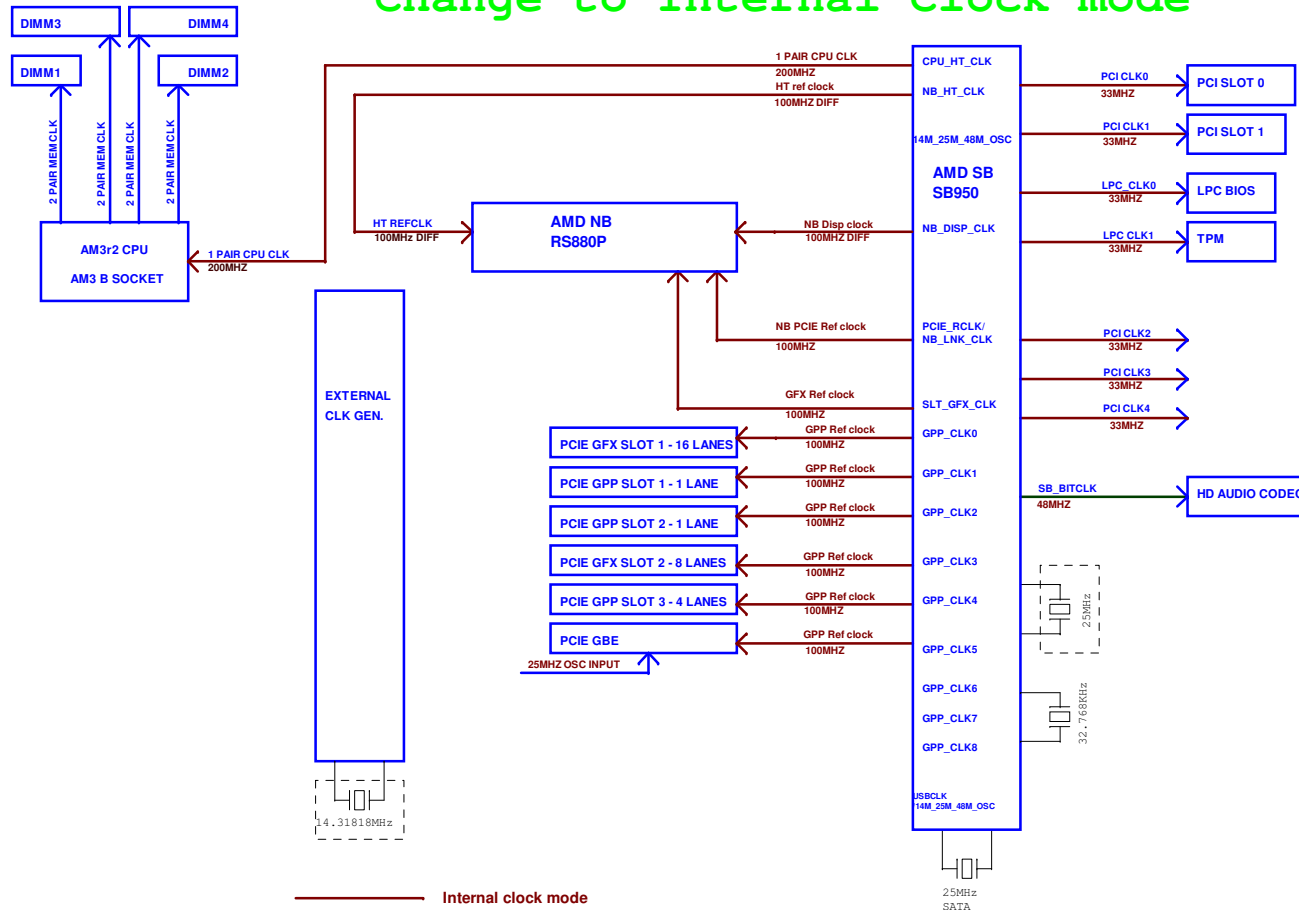
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RS880P + SB950 Power Delivery Architecture



2010/10/9 Change to Internal Clock mode



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hei Tai Wu Rd
Hsichih, Taipei

Title

CLOCK MAP

Size

Document Number

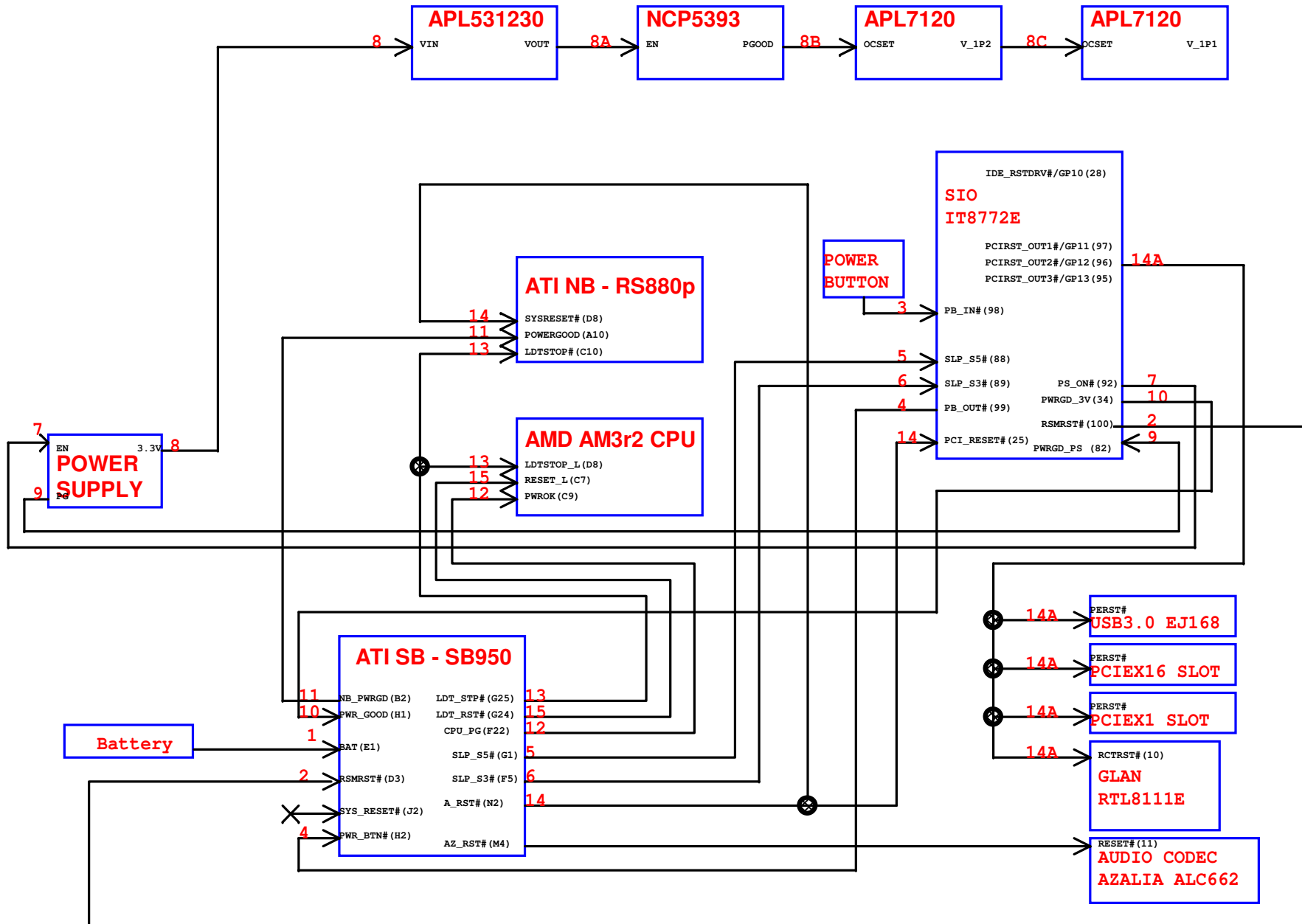
NADIA

Rev

SA

Date: Thursday, March 31, 2011

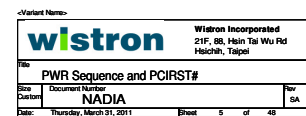
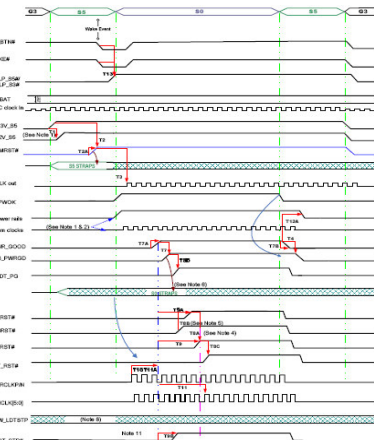
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RESET/POWER GOOD MAP

RSMRST

Del Discrete RSMRST circuit



Pin Name	Pin#	GPIO Type	POWER VELL	Default Func	Default State	USAGE (BUT label)	Strap	IO	S2	S4	S5	SET	Notes
A00SGR00	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A01SGP01	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A02SGP02	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A03SGP03	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A04SGP04	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A05SGP05	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A06SGP06	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A07SGP07	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A08SGP08	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A09SGP09	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A10SGP10	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A11SGP11	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A12SGP12	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A13SGP13	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A14SGP14	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A15SGP15	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A16SGP16	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A17SGP17	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A18SGP18	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A19SGP19	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A20SGP20	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A21SGP21	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A22SGP22	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A23SGP23	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A24SGP24	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A25SGP25	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A26SGP26	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A27SGP27	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A28SGP28	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A29SGP29	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A30SGP30	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A31SGP31	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A32SGP32	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A33SGP33	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A34SGP34	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A35SGP35	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A36SGP36	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A37SGP37	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A38SGP38	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A39SGP39	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							
A40SGP40	A481	IO	3.3V I/O (Vcc) (Vcc)	PO	Output HIGH	no use							

PWR NAME	PWR	GPO TYPE	POWER VELL	Default Func	Default State	USAGE (NET name)	Strap	S0	S3	S4	S5	SET	Notes
AS11GPO001	A60	IO	3.3V I-S/V tolerance	PGU	Output High	no use						GPO High	
AS11GPO002	A60	IO	3.3V I-S/V tolerance	PGU	Input	Input 3.3V I-V						GPO High	
INTGPG001	A60	IO	3.3V I-S/V tolerance	PGU	Input 3.3V I-V	no use						GPO High	
AS11GPO003	A60	IO	3.3V I-S/V tolerance	PGU	Input 3.3V I-V	no use						GPO High	
INTGPG002	A14	IO	3.3V I-S/V tolerance	PGU	Input 3.3V I-V	no use						GPO High	
PGCLKGPO001	U1	O	3.3V I-S/V tolerance	PGCLK	Output	PGU CLK13	Low					OBSS	10k to V3
PGCLKGPO002	U1	O	3.3V I-S/V tolerance	PGCLK	Output	PGU CLK13	Low					OBSS	10k to GND
PGCLKGPO003	U1	O	3.3V I-S/V tolerance	PGCLK	Output	PGU CLK13	Low					OBSS	10k to V3
PGCLKGPO004	U1	O	3.3V I-S/V tolerance	PGCLK	Output	PGU CLK13	High					OBSS	10k to V3
REQ10GPO001	AHS	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO002	AHS	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO003	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO004	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO005	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO006	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO007	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO008	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO009	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO010	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO011	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO012	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO013	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO014	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO015	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO016	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO017	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO018	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO019	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO020	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO021	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO022	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO023	A12	IO	3.3V I-S/V tolerance	PGU	Input 15K I-V	no use						GPO High	
REQ10GPO024	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO025	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO026	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO027	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO028	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO029	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO030	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO031	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO032	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO033	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO034	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO035	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO036	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO037	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO038	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO039	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO040	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO041	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO042	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO043	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO044	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO045	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO046	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO047	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO048	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO049	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO050	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO051	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO052	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO053	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO054	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
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REQ10GPO063	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO064	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO065	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO066	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO067	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO068	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO069	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO070	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO071	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
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REQ10GPO074	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO075	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO076	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO077	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO078	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO079	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO080	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO081	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO082	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO083	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO084	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO085	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO086	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO087	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO088	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO089	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO090	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO091	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO092	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO093	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO094	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO095	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO096	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO097	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO098	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO099	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	
REQ10GPO100	V9	IO	3.3V	PGU	Input 3.3V I-V	no use						GPO High	

	CLK_REC0FAMU4GPO62	AH21	I/O	3.3V (±5-V tolerance)	null	input, 0.2K Pu	no use	GPO_High
	CLK_REC0SATA_STINGP083	AA16	I/O	3.3V (±5-V tolerance)	null	input, 0.2K Pu	#F_AUDIO_PREFERENCE?	
	CLK_REC0SATA_SINGP090A	AD19	I/O	3.3V (±5-V tolerance)	null	input, 0.2K Pu	BSP_020	GPO_Low
	CLK_REC0SATA_SINGP090B	AA25	I/O	3.3V (±5-V tolerance)	null	input, 0.2K Pu	BLAUDIO_RX_CLK_IL1	
	CLK_REC0SDIO_SPDGRSS007EEDITE# SPMGRSS000	AF19	I/O	3.3V (±5-V tolerance)	null	To-State SB_SPDR	S8_SPDR	10k to V _P S58 1k to GND
	SATA_ACTWGDMDI	AD11	O/D	3.3V	null	input, To-State Ldr*	ICH SATA_LFR*	10k to V _P , 3PA

[illegible][illegible][illegible]

Notes: Z = Tri-state, IO = Bidirectional, I = Input, O = Output, OD = Open Drain, OC = Open Collector, U = Unpowered, L = Low, H=High

[illegible]

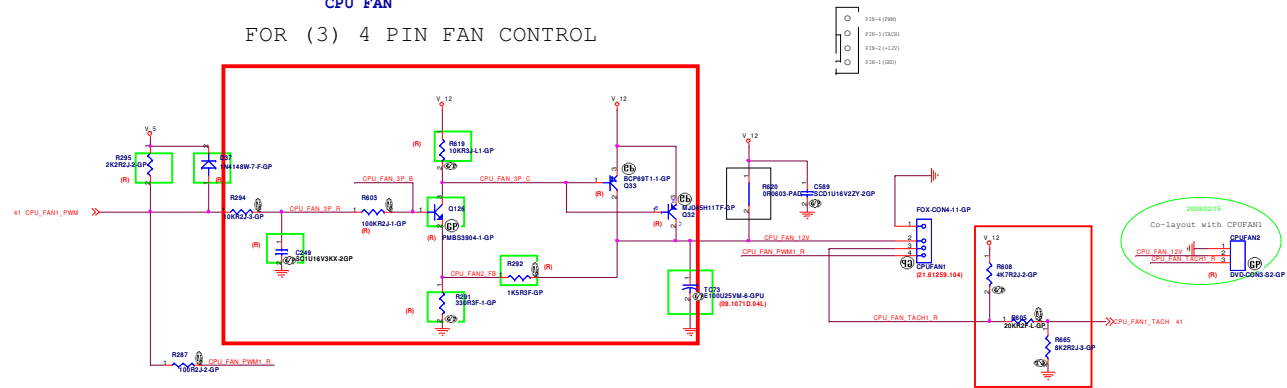
CPU FAN

41 CPU_FAN1_PWM >>>
41 CPU_FAN1_TACH <<<

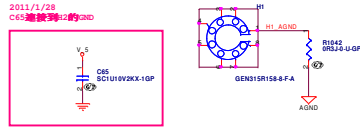
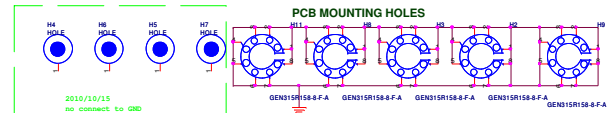
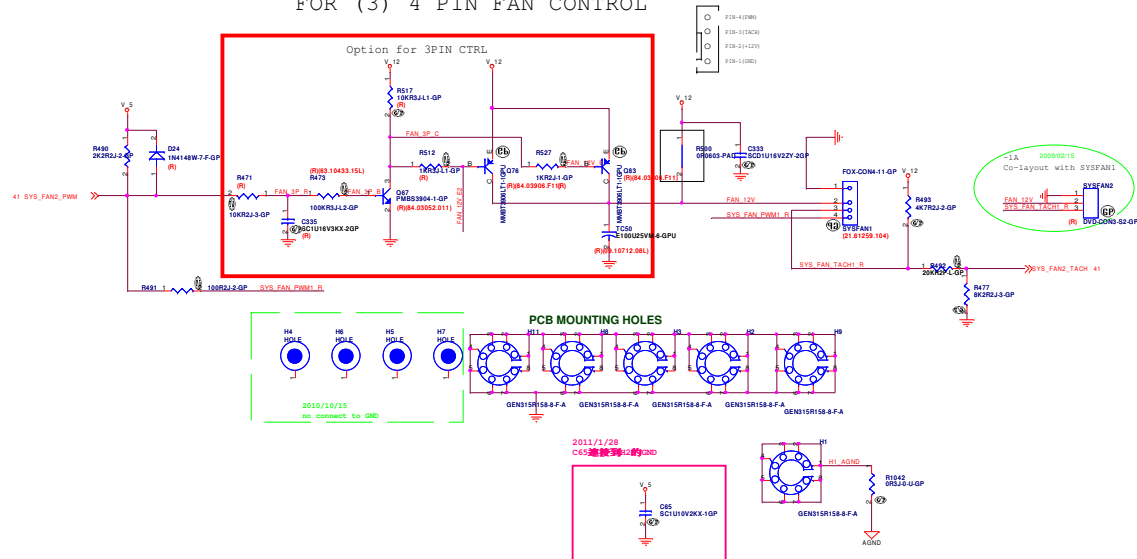
SYS FAN

41 SYS_FAN2_PWM >>>
41 SYS_FAN2_TACH <<<


CPU FAN FOR (3) 4 PIN FAN CONTROL



SYS FAN FOR (3) 4 PIN FAN CONTROL



2010/10/7
Delete External Clock Generator

<Variant Name>	
 Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title EXTERNAL CLOCK GENERATOR	
Size Custom	Document Number NADIA
Date: Thursday, March 31, 2011	Rev SA
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HT Interface

15 HT_CLKIN1_P >> HT_CLKIN1_P
15 HT_CLKIN1_N >> HT_CLKIN1_N
15 HT_CLKIN0_P >> HT_CLKIN0_P
15 HT_CLKIN0_N >> HT_CLKIN0_N

15 HT_CTLIN1_P >> HT_CTLIN1_P
15 HT_CTLIN1_N >> HT_CTLIN1_N
15 HT_CTLIN0_P >> HT_CTLIN0_P
15 HT_CTLIN0_N >> HT_CTLIN0_N

15 HT_CLKOUT1_P << HT_CLKOUT1_P
15 HT_CLKOUT1_N << HT_CLKOUT1_N
15 HT_CLKOUT0_P << HT_CLKOUT0_P
15 HT_CLKOUT0_N << HT_CLKOUT0_N

15 HT_CTLOUT1_P << HT_CTLOUT1_P
15 HT_CTLOUT1_N << HT_CTLOUT1_N
15 HT_CTLOUT0_P << HT_CTLOUT0_P
15 HT_CTLOUT0_N << HT_CTLOUT0_N

15 HT_CADIN7_P >> HT_CADIN7_P
15 HT_CADIN7_N >> HT_CADIN7_N
15 HT_CADIN6_P >> HT_CADIN6_P
15 HT_CADIN6_N >> HT_CADIN6_N
15 HT_CADIN5_P >> HT_CADIN5_P
15 HT_CADIN5_N >> HT_CADIN5_N
15 HT_CADIN4_P >> HT_CADIN4_P
15 HT_CADIN4_N >> HT_CADIN4_N
15 HT_CADIN3_P >> HT_CADIN3_P
15 HT_CADIN3_N >> HT_CADIN3_N
15 HT_CADIN2_P >> HT_CADIN2_P
15 HT_CADIN2_N >> HT_CADIN2_N
15 HT_CADIN1_P >> HT_CADIN1_P
15 HT_CADIN1_N >> HT_CADIN1_N
15 HT_CADIN0_P >> HT_CADIN0_P
15 HT_CADIN0_N >> HT_CADIN0_N

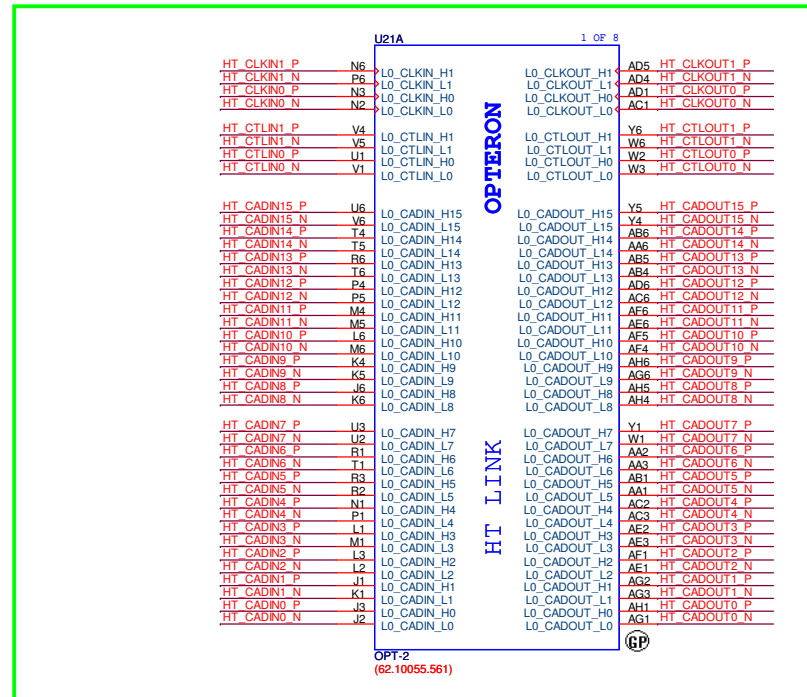
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15 HT_CADIN14_P >> HT_CADIN14_P
15 HT_CADIN14_N >> HT_CADIN14_N
15 HT_CADIN13_P >> HT_CADIN13_P
15 HT_CADIN13_N >> HT_CADIN13_N
15 HT_CADIN12_P >> HT_CADIN12_P
15 HT_CADIN12_N >> HT_CADIN12_N
15 HT_CADIN11_P >> HT_CADIN11_P
15 HT_CADIN11_N >> HT_CADIN11_N
15 HT_CADIN10_P >> HT_CADIN10_P
15 HT_CADIN10_N >> HT_CADIN10_N
15 HT_CADIN9_P >> HT_CADIN9_P
15 HT_CADIN9_N >> HT_CADIN9_N
15 HT_CADIN8_P >> HT_CADIN8_P
15 HT_CADIN8_N >> HT_CADIN8_N

15 HT_CADOUT7_P << HT_CADOUT7_P
15 HT_CADOUT7_N << HT_CADOUT7_N
15 HT_CADOUT6_P << HT_CADOUT6_P
15 HT_CADOUT6_N << HT_CADOUT6_N
15 HT_CADOUT5_P << HT_CADOUT5_P
15 HT_CADOUT5_N << HT_CADOUT5_N
15 HT_CADOUT4_P << HT_CADOUT4_P
15 HT_CADOUT4_N << HT_CADOUT4_N
15 HT_CADOUT3_P << HT_CADOUT3_P
15 HT_CADOUT3_N << HT_CADOUT3_N
15 HT_CADOUT2_P << HT_CADOUT2_P
15 HT_CADOUT2_N << HT_CADOUT2_N
15 HT_CADOUT1_P << HT_CADOUT1_P
15 HT_CADOUT1_N << HT_CADOUT1_N
15 HT_CADOUT0_P << HT_CADOUT0_P
15 HT_CADOUT0_N << HT_CADOUT0_N

15 HT_CADOUT15_P << HT_CADOUT15_P
15 HT_CADOUT15_N << HT_CADOUT15_N
15 HT_CADOUT14_P << HT_CADOUT14_P
15 HT_CADOUT14_N << HT_CADOUT14_N
15 HT_CADOUT13_P << HT_CADOUT13_P
15 HT_CADOUT13_N << HT_CADOUT13_N
15 HT_CADOUT12_P << HT_CADOUT12_P
15 HT_CADOUT12_N << HT_CADOUT12_N
15 HT_CADOUT11_P << HT_CADOUT11_P
15 HT_CADOUT11_N << HT_CADOUT11_N
15 HT_CADOUT10_P << HT_CADOUT10_P
15 HT_CADOUT10_N << HT_CADOUT10_N
15 HT_CADOUT9_P << HT_CADOUT9_P
15 HT_CADOUT9_N << HT_CADOUT9_N
15 HT_CADOUT8_P << HT_CADOUT8_P
15 HT_CADOUT8_N << HT_CADOUT8_N

2010/11/11

Change CPU socket to 62.10055.561



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CPU HT Interface			
Size A3	Document Number NADIA		Rev SA
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```

2010/10/6
CLK from SB to CPU

```

```

28 SB_CPU_CLKIN_P  >>> SB_CPU_CLKIN_P
28 SB_CPU_CLKIN_N  >>> SB_CPU_CLKIN_N

```

28 CPUPWRGD_R <== CPUPWRGD_R
17,28 LDT_STOP# <== LDT_STOP#
28 LDT_RST# <== LDT_RST#

29,41 CPU_SiC <== CPU_SiC
29,41 CPU_SiD <== CPU_SiD

47 CPU_CORE_FB <== CPU_CORE_FB
47 CPU_CORE_FB* <== CPU_CORE_FB*

```

47 CPU_VID5 CPU_VID5
47 CPU_VID4 CPU_VID4
47 CPU_VID3/SVC CPU_VID3/SVC
47 CPU_VID2/SVD CPU_VID2/SVD
47 CPU_VID1/SEL CPU_VID1/SEL
47 CPU_VID0 CPU_VID0

```

```

5.29 CPU_THERMTRIP# SB << CPU_THERMTRIP# SB
28 CPU_PROCHOT# SB << CPU_PROCHOT# SB

47 CPU_NB_FB_P << CPU_NB_FB_P
47 CPU_NB_FB_N << CPU_NB_FB_N

47 CPU_PSI* << CPU_PSI*

```

47 CPU_NB_FB_P << CPU_NB_FB_P
47 CPU_NB_FB_N << CPU_NB_FB_N

30. T_ALERT# // T_ALERT#

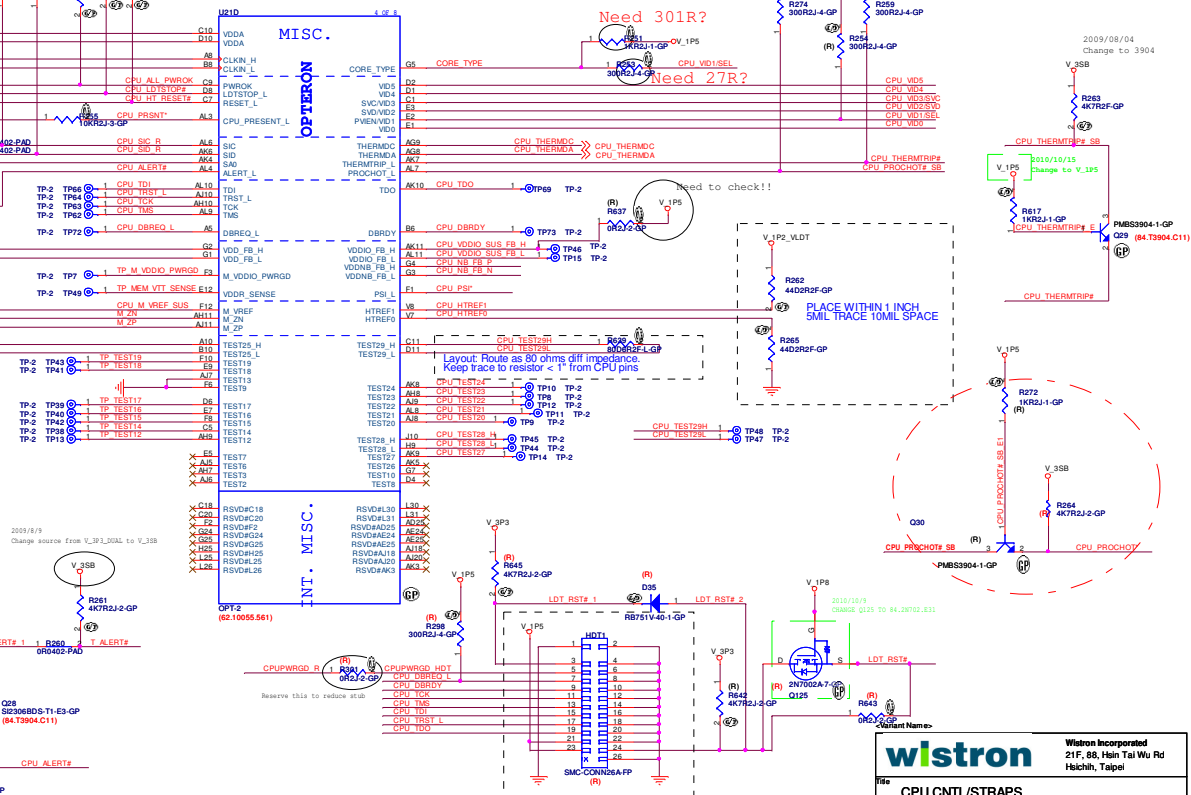
[illegible]

2010/11/19
EMI suggestion

CPU HT RESET# 2011/3/9
Delete C210 for power sequence

[illegible]

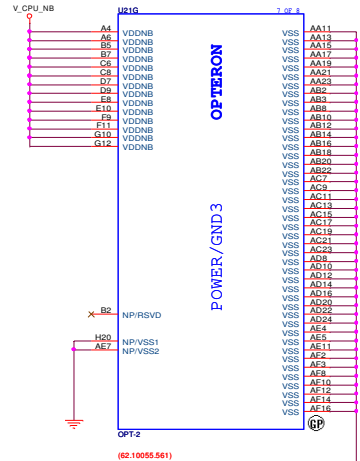
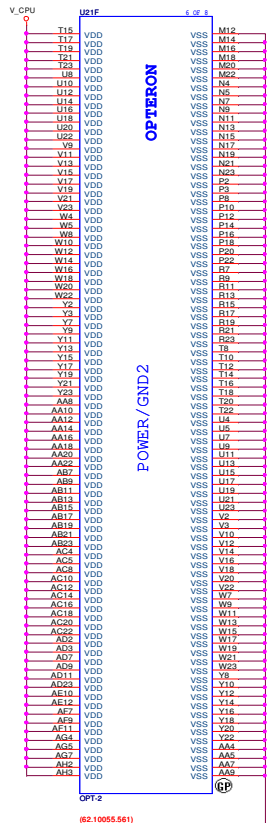
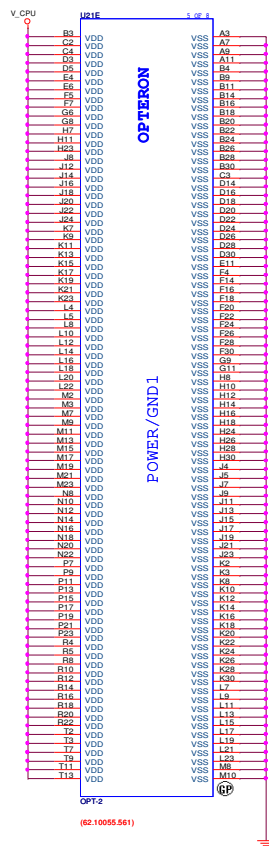
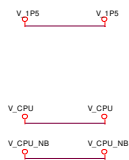
Change CPU socket to 62.10055.561



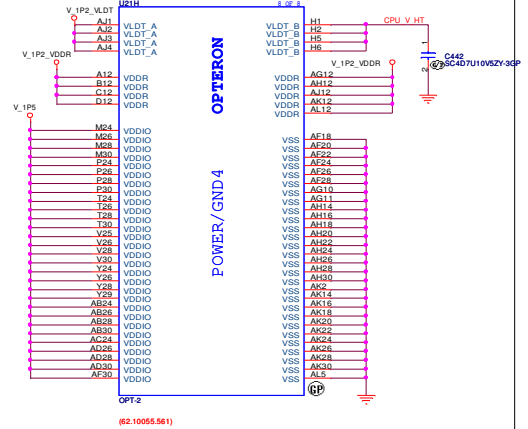
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Title CPU CNTL/STRAPS	
Size Custom	Document Number NADIA
Date Thursday March 21, 2011	Sheet 10 of 48 Rev SA



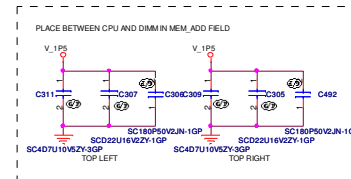
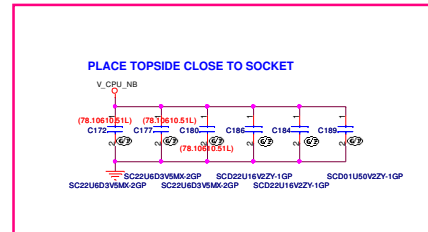
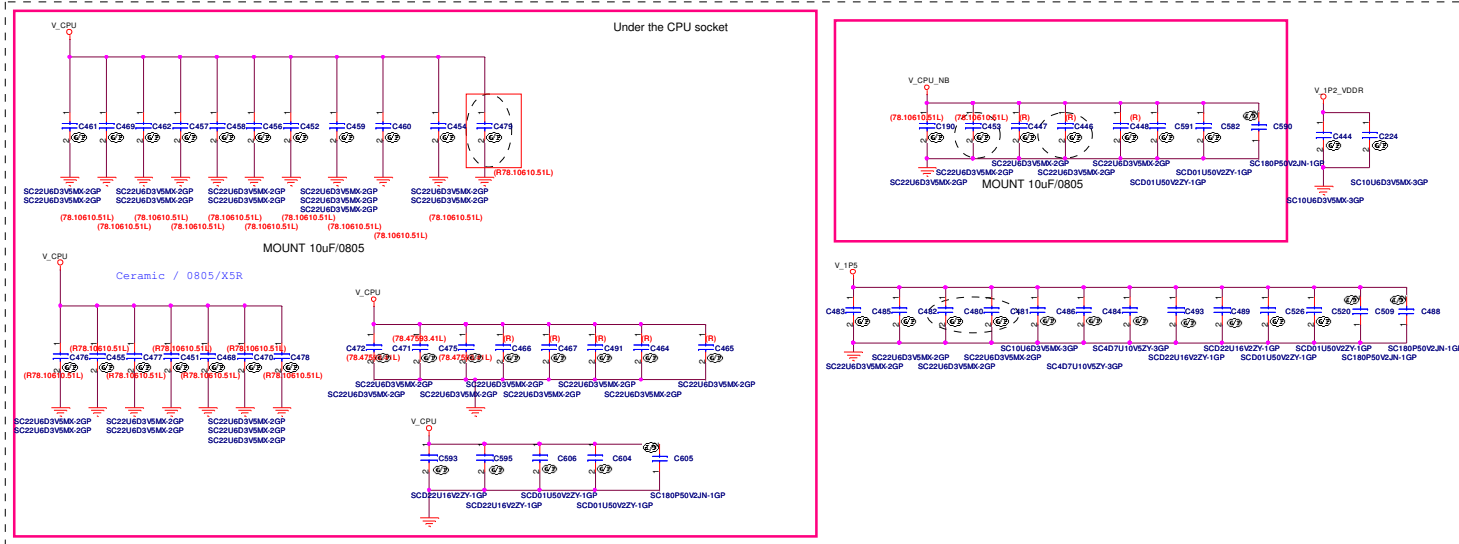
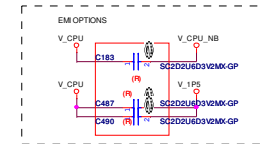
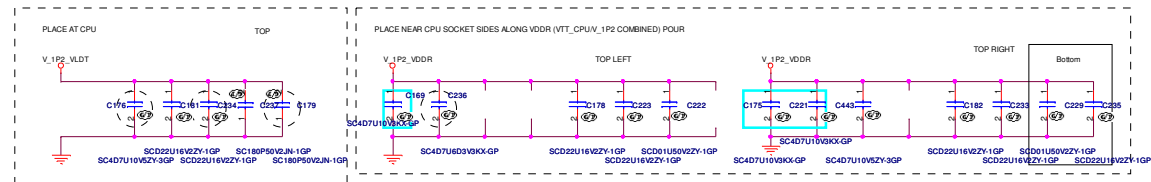
POWER




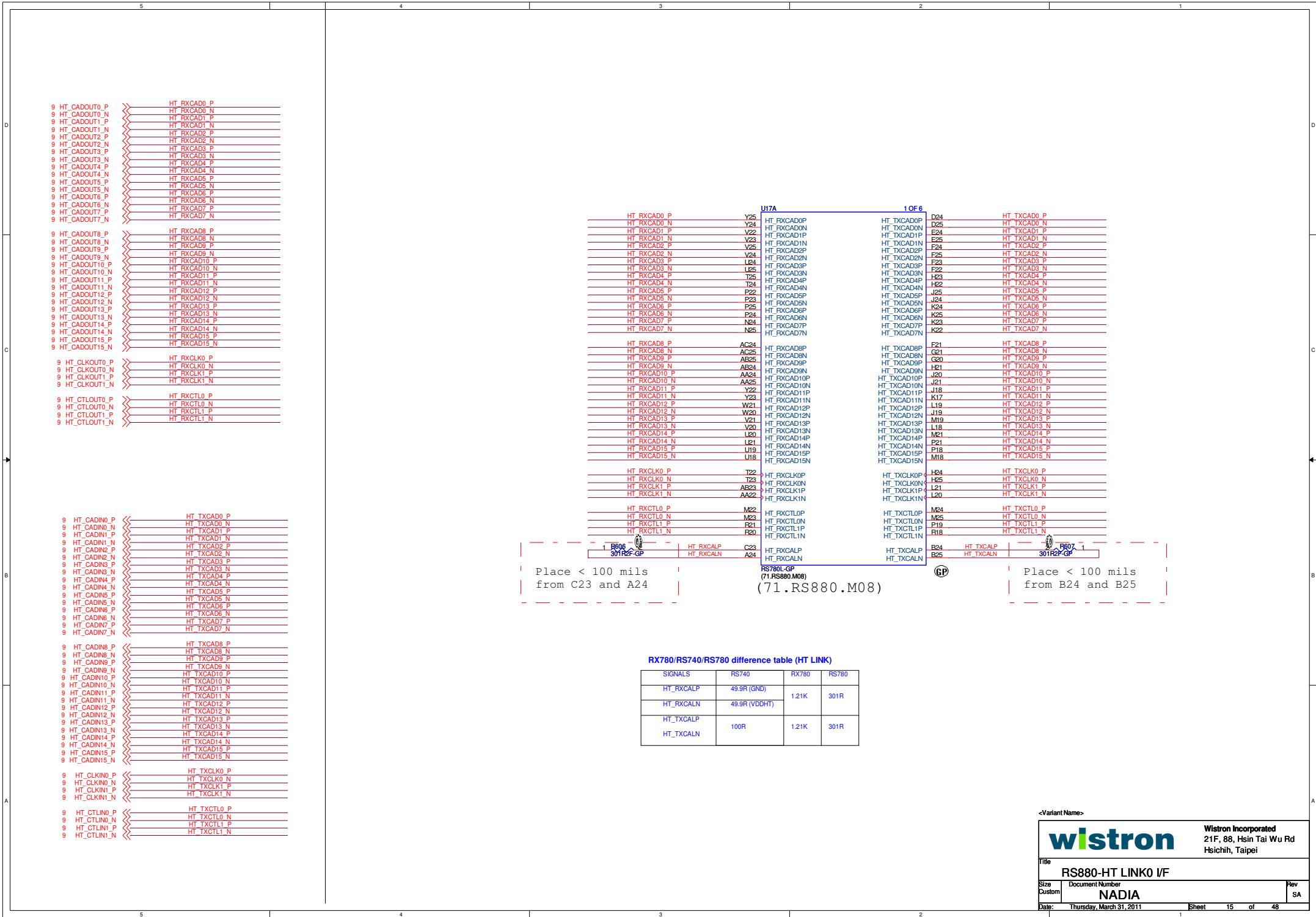
Either VLDT_A or VLDT_B is connected to V_IP2

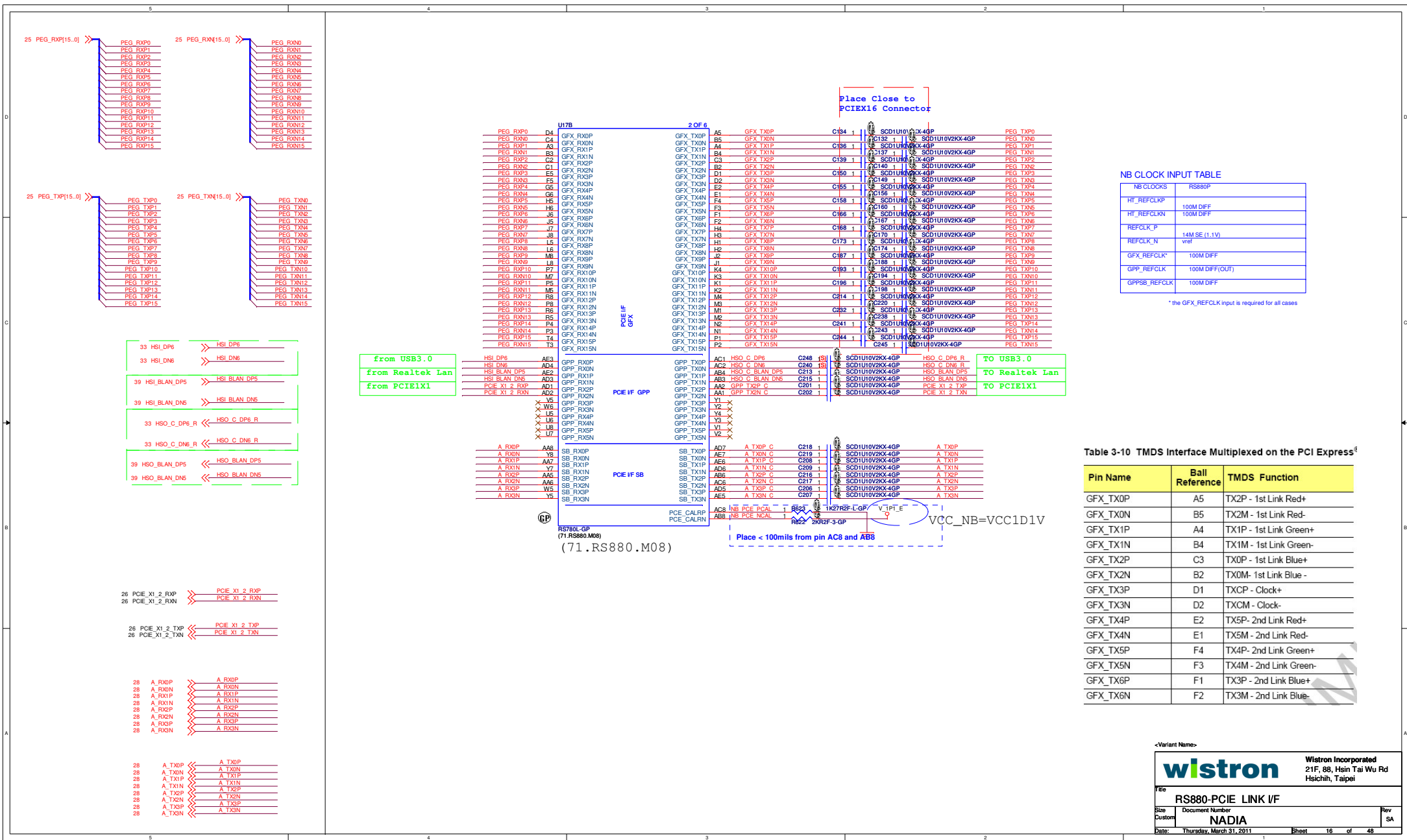


2010/11/11
Change CPU socket to 62.10055.561



		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CPU DECOUPLING			
Size Custom	Document Number NADIA		Rev SA
Date: Thursday, March 31, 2011		Sheet 14 of 48	





NB CLOCK INPUT TABLE	
NB CLOCKS	RS880P
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	wref
GFX_REFCLK*	100M DIFF
GPP_REFCLK	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF

* the GFX_REFCLK input is required for all cases

Table 3-10 TMDs Interface Multiplexed on the PCI Express®

Pin Name	Ball Reference	TMDs Function
GFX_TX0P	A5	TX2P - 1st Link Red+
GFX_TX0N	B5	TX2M - 1st Link Red-
GFX_TX1P	A4	TX1P - 1st Link Green+
GFX_TX1N	B4	TX1M - 1st Link Green-
GFX_TX2P	C3	TX0P - 1st Link Blue+
GFX_TX2N	B2	TX0M - 1st Link Blue -
GFX_TX3P	D1	TXCP - Clock+
GFX_TX3N	D2	TXCM - Clock-
GFX_TX4P	E2	TX5P- 2nd Link Red+
GFX_TX4N	E1	TX5M - 2nd Link Red-
GFX_TX5P	F4	TX4P- 2nd Link Green+
GFX_TX5N	F3	TX4M - 2nd Link Green-
GFX_TX6P	F1	TX3P - 2nd Link Blue+
GFX_TX6N	F2	TX3M - 2nd Link Blue-

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File

RS880-PCIE LINK V/F

Size

Document Number

Rev

SA

Customer

NADIA

Date

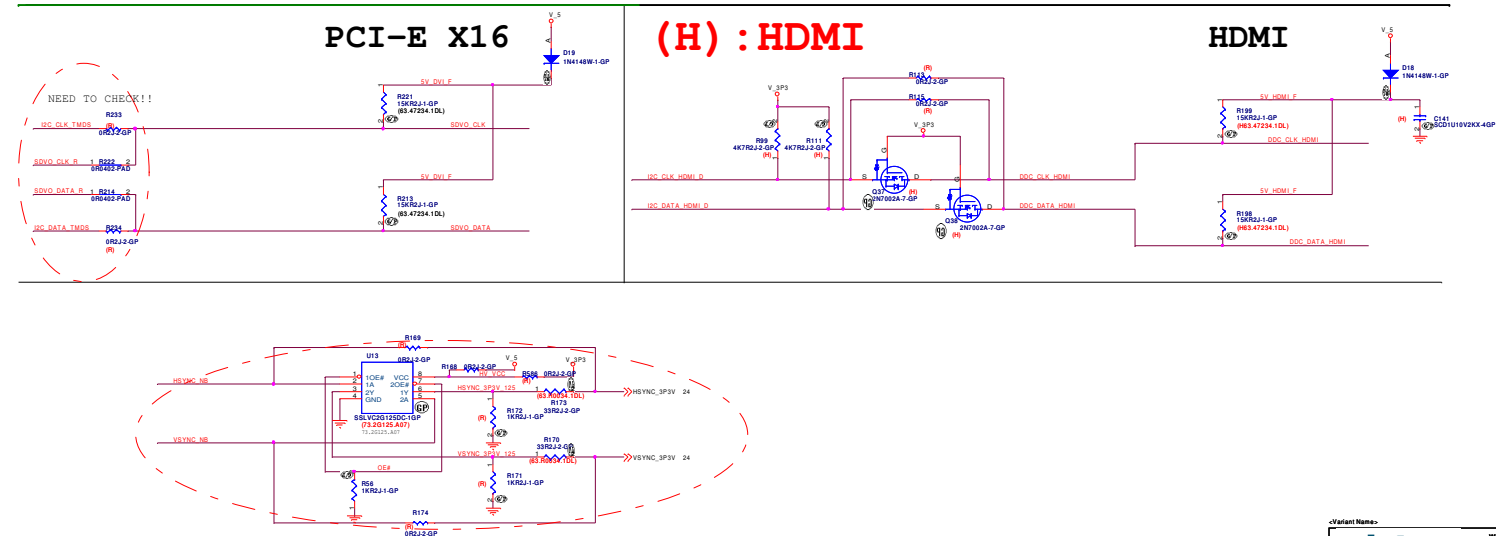
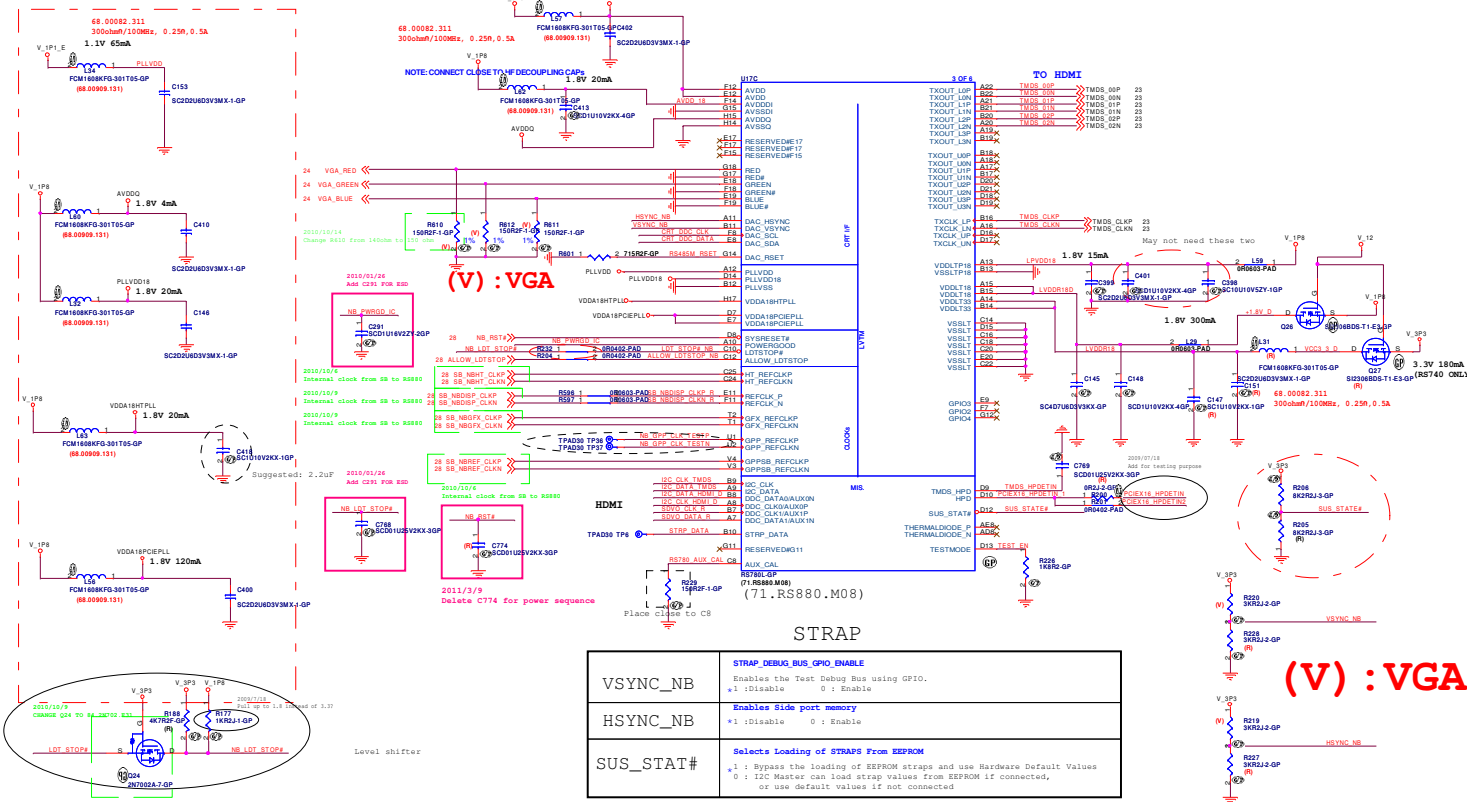
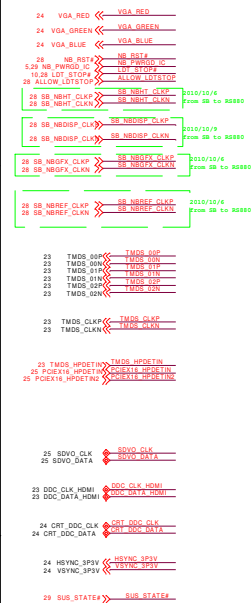
Thursday, March 31, 2011

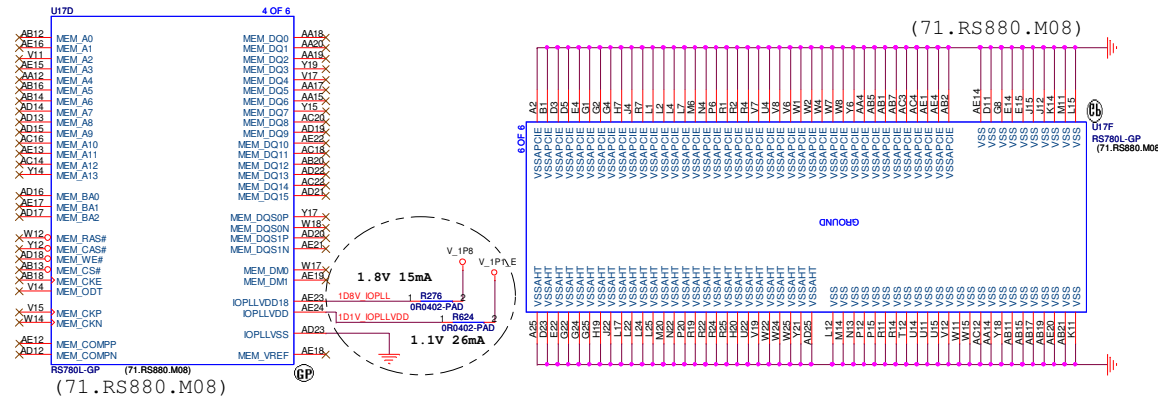
Sheet

16

of

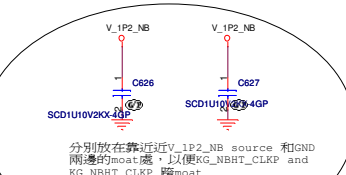
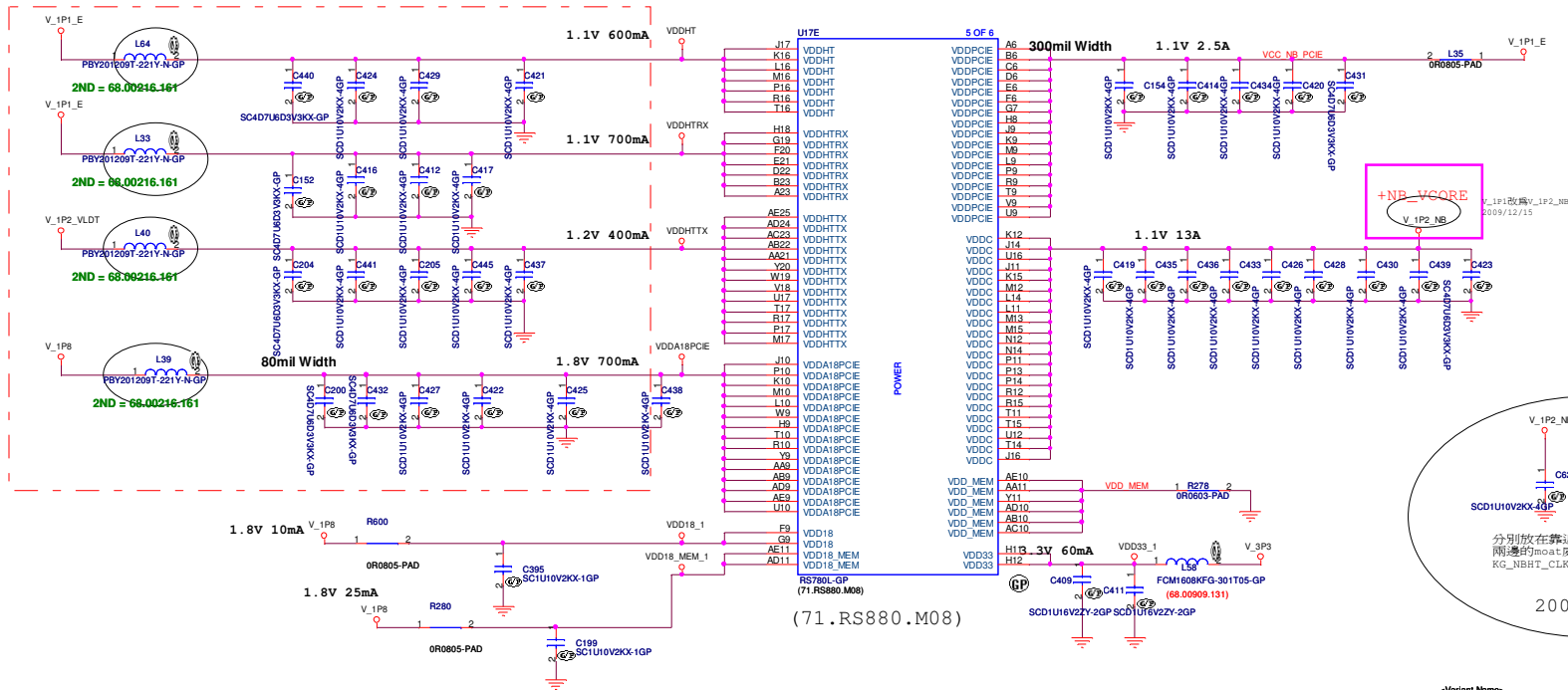
48

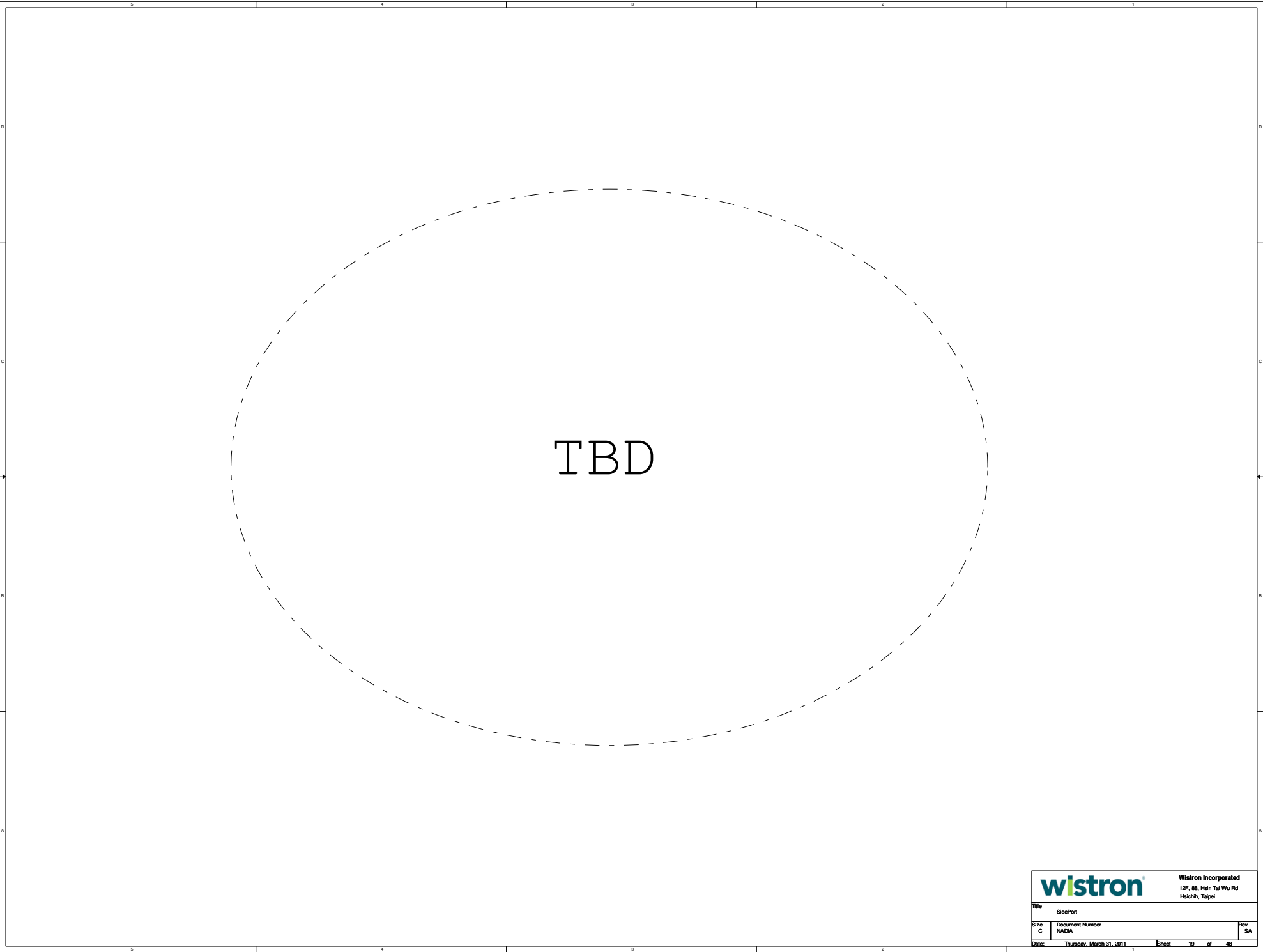


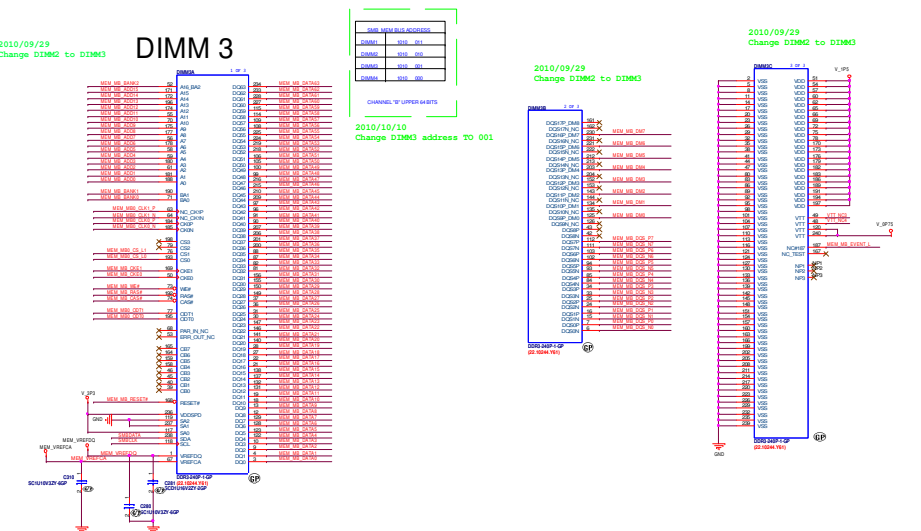
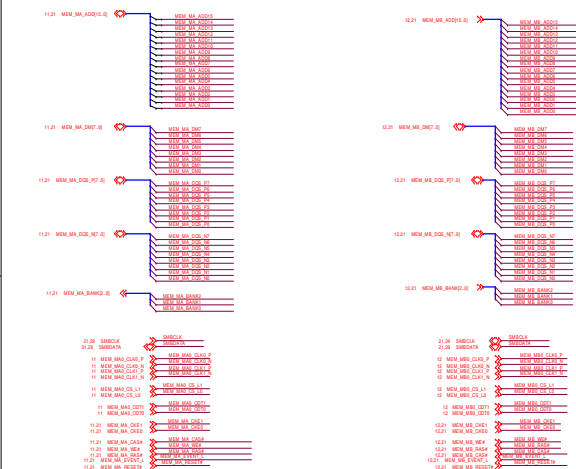


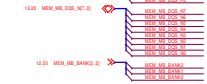
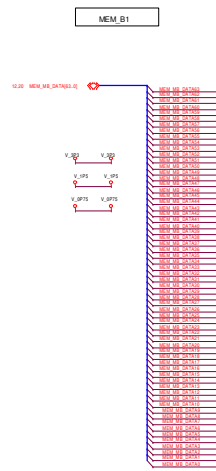
RS880P POWER DIFFERENCE TABLE

PIN NAME	POWER	PIN NAME	POWER
AVDD	+3.3V	VDDA18PCIEPLL	+1.8V
AVDDDI	+1.8V	VDDC	+1.2V
AVDDQ	+1.8V	VDDI8	+1.8V
IOPLLVD	+1.1V	VDDQ3	+3.3V
IOPLLVDI8	+1.8V	VDDHT	+1.1V
PLLVD	+1.1V	VDDHTRX	+1.1V
PLLVDI8	+1.8V	VDDHTTX	+1.2V
VDD_MEM	+1.8V(DDR2)	VDDL18	+1.8V
VDDI8_MEM	+1.5V(DDR3)	VDDLTP18	+1.8V
VDDA18HTPLL	+1.8V	VDDPCIE	+1.1V
VDDA18PCIE	+1.8V		

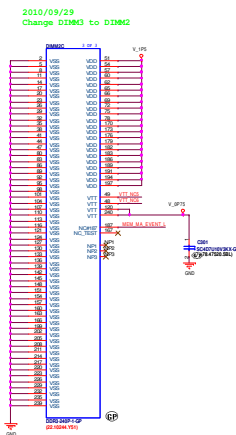






[illegible]

2010/10/10
Change DIMM2 address TO 010

[illegible]

2010/09/29
Change DIMM4 to DIMM1

2010/10/10
Change DIMM1 address TO 011

Diagram illustrating a 2D array structure, labeled "DMM16" and "2D". The array is organized into four groups of four rows each, labeled "DMM16" on the left. The elements are labeled with coordinates (row, column) in the format "DMM16 (row, column)".

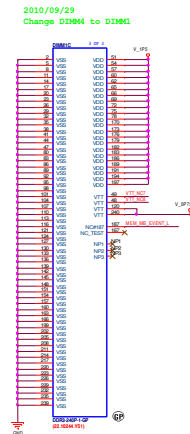
The first group of four rows is labeled "DMM16 (0, 0)" to "DMM16 (3, 3)".

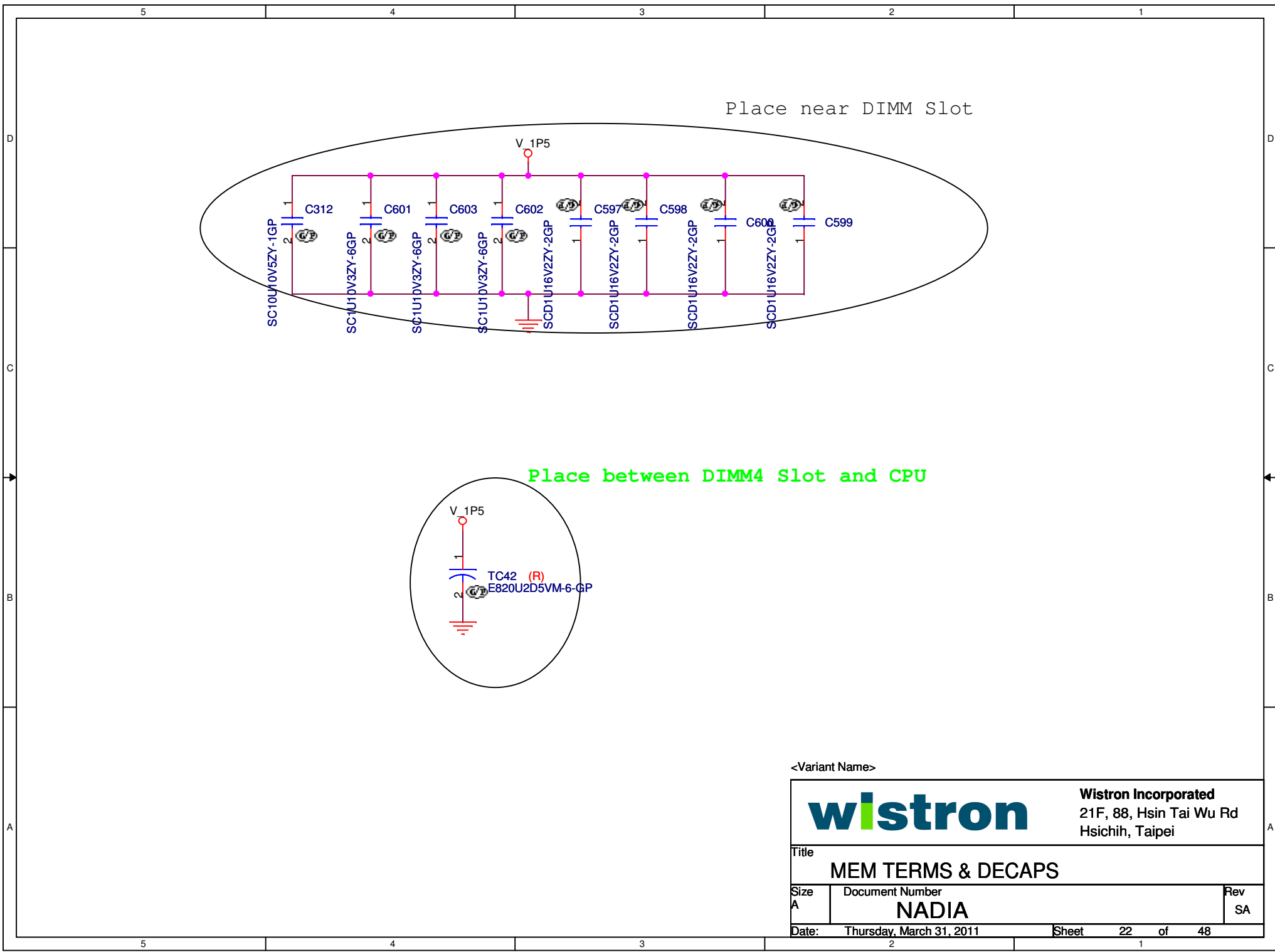
The second group of four rows is labeled "DMM16 (4, 0)" to "DMM16 (7, 3)".

The third group of four rows is labeled "DMM16 (8, 0)" to "DMM16 (11, 3)".


The fourth group of four rows is labeled "DMM16 (12, 0)" to "DMM16 (15, 3)".

The array is also labeled "DMM16" at the bottom left and "2D" at the bottom right.





<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title MEM TERMS & DECAPS			
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(H) : HDMI

DDC

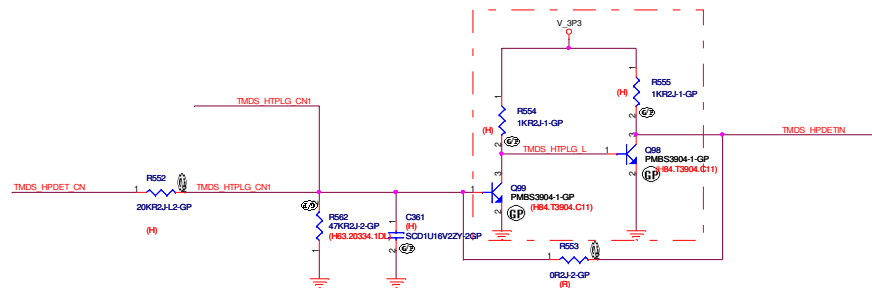
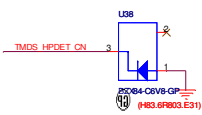
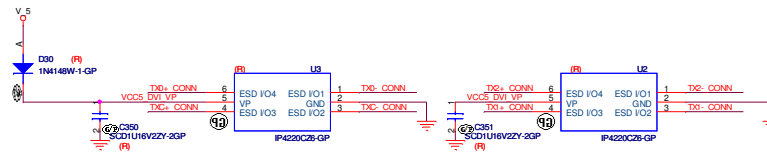
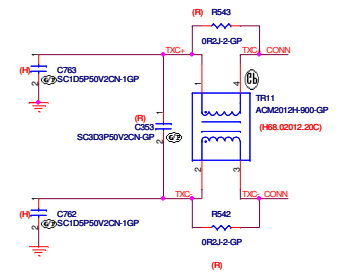
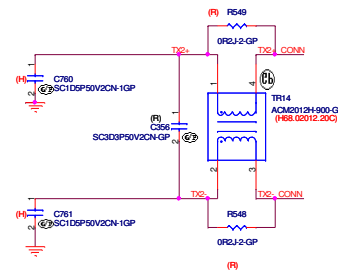
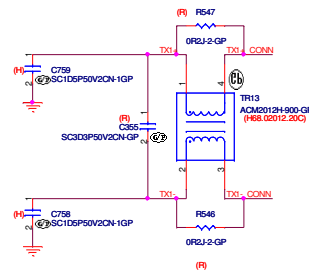
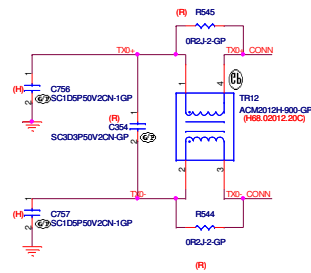
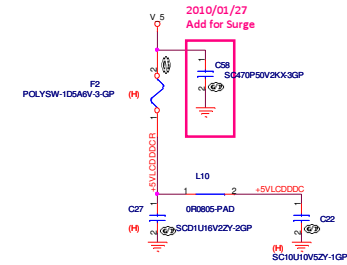
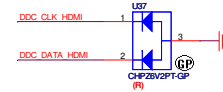
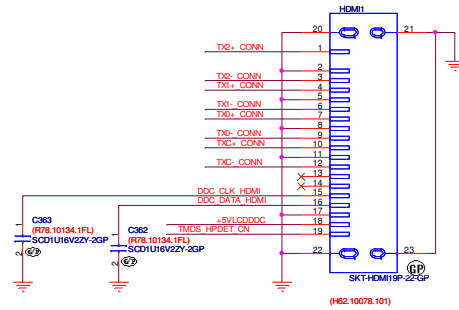
- 17 DDC_CLK_HDMI
- 17 DDC_DATA_HDMI

CLK DATA

- 17 TMDS_CLKN TXC-
- 17 TMDS_CLKP TXC+
- 17 TMDS_D0N TXD-
- 17 TMDS_D0P TXD+
- 17 TMDS_D1N TX1-
- 17 TMDS_D1P TX1+
- 17 TMDS_D2N TX2-
- 17 TMDS_D2P TX2+

TMDS HPD

- 17 TMDS_HPDETIN



CLOSED TO HDMI CONNECTOR

-Variant Name-			
wistron			
Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsinchu, Taipei			
HDMI CONN			
File	Document Number	Rev	
Size	NADIA	SA	
Custom			
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Video Filter

(V) : VGA

Place PI filter close to VGA connector
5 mil trace width/20 mil spacing

RGB

17 VGA_RED >>
17 VGA_GREEN >>
17 VGA_BLUE >>

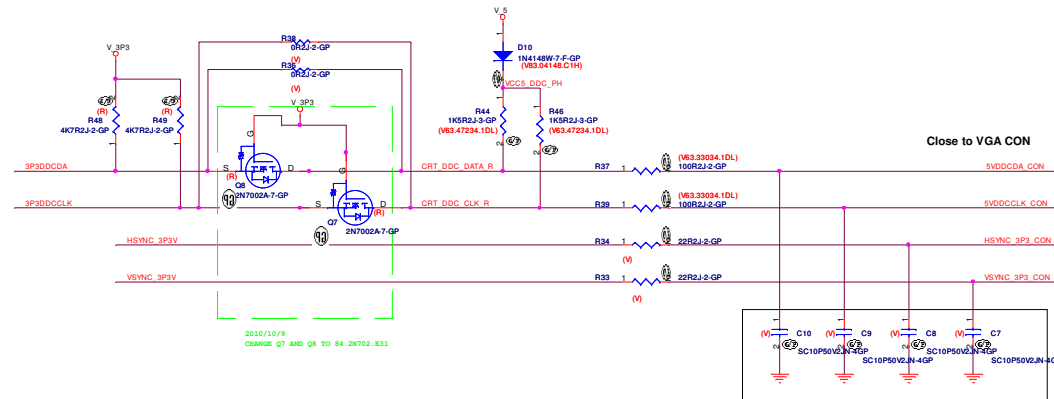
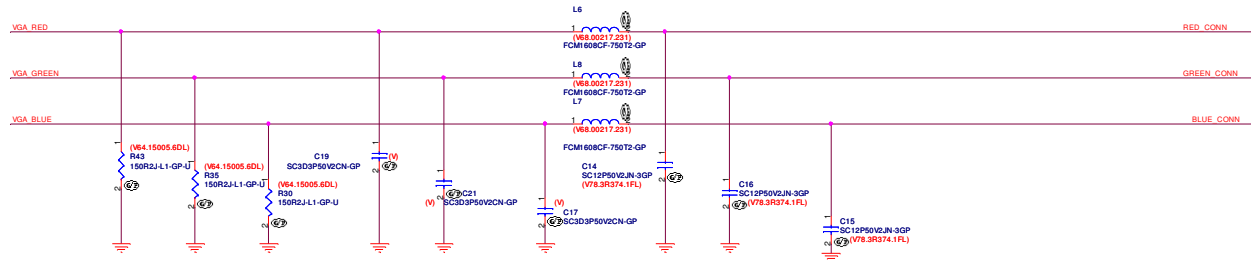
H&V_SYNC

17 HSYNC_3P3V >>
17 VSYNC_3P3V >>

DDC

17 CRT_DDC_CLK >>
17 CRT_DDC_DATA >>

2009/8/9
Swap the wrong connections of VGA_DDC/CLK

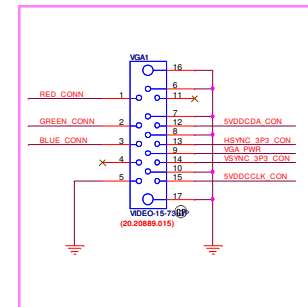
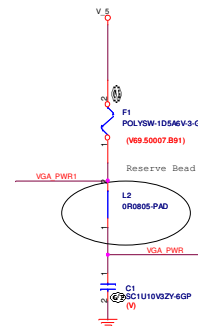
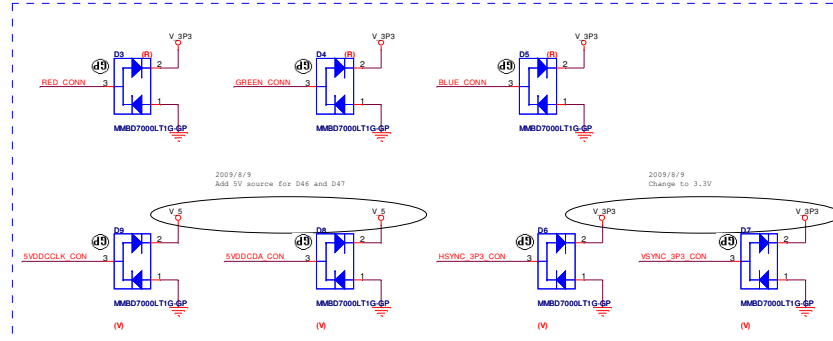


Close to VGA CON

34.00015.231 x 2
Screw for VGA connector
(No need for 20.20825.015)

2011/02/08
Change VGA1 to 20.20889.015

2009/07/02



<Variant Name>

wlstron
Wistron Incorporated
21F, 88, Hei Tai Wu Rd
Hsinchu, Taipei

Title		VGA CONN	
Rev	Document Number	Rev	SA
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SRC Clocks

28 SB_GFX_S0_CLKP >> SB_GFX_S0_CLKP
28 SB_GFX_S0_CLKN >> SB_GFX_S0_CLKN

PCIeX16

TX signals

16 PEG_TXN[15..0] << EXP_16X_TXN[15..0]
16 PEG_TXN[15..0] << EXP_16X_TXN[15..0]

RX signals

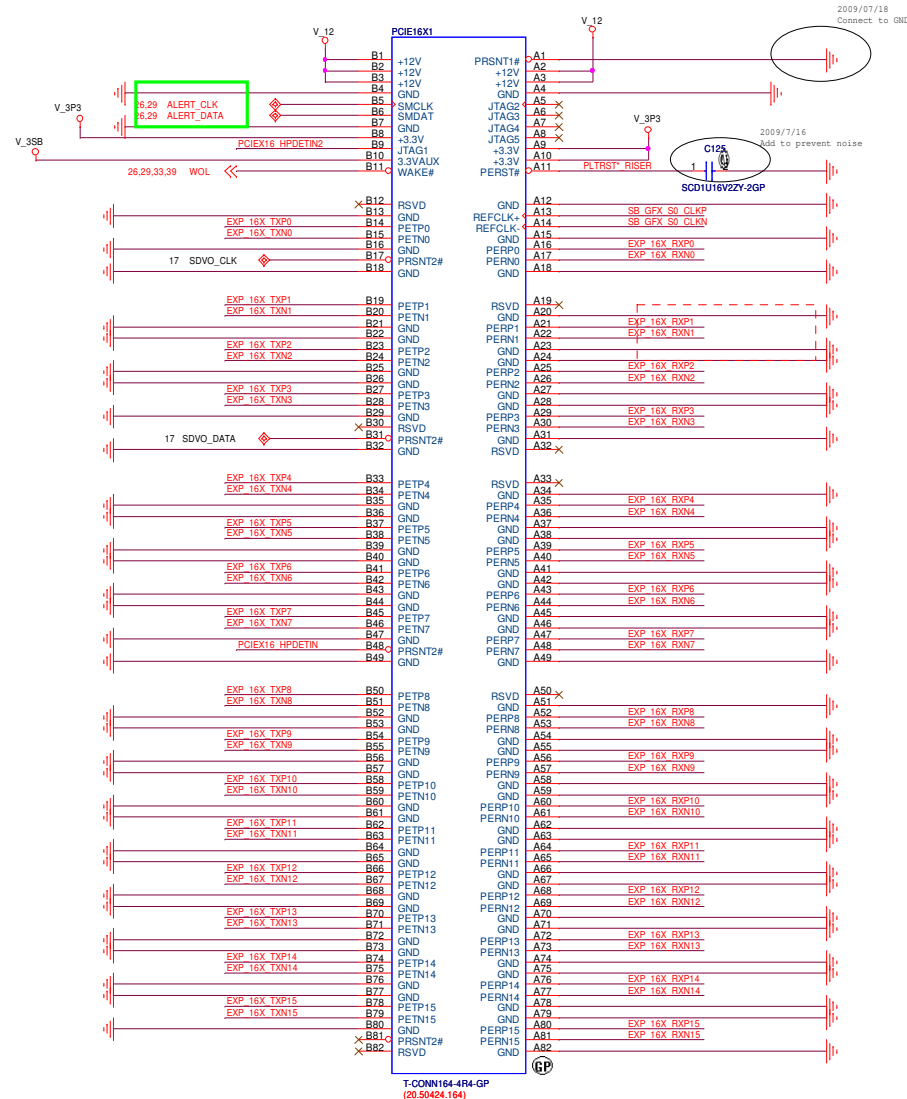
16 PEG_RXP[15..0] << EXP_16X_RXP[15..0]
16 PEG_RXN[15..0] << EXP_16X_RXN[15..0]

SMBUS

26,29 ALERT_CLK <<
26,29 ALERT_DATA <<

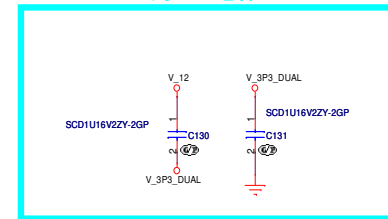
MISC

26,29,33,39 WOL <<
17 SDVO_CLK <<
17 SDVO_DATA <<
26,28 PLTRST*_RISER >>
17 PCIE16_HPDETIN << PCIE16_HPDETIN
17 PCIE16_HPDETIN2 << PCIE16_HPDETIN2

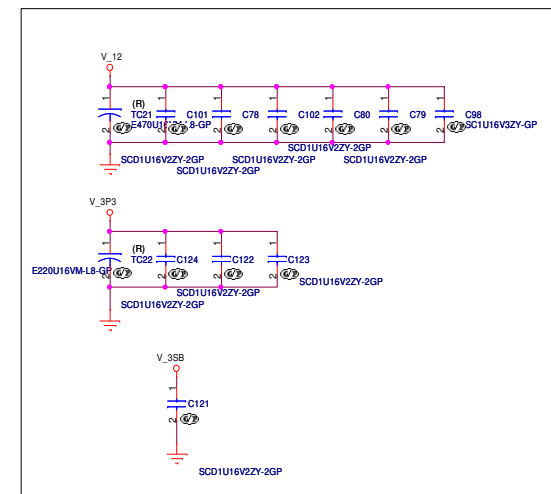


2010/11/29

Add 跨Moat電容



PLACE CAPS NEAR PCI-Ex16 CONNECTORS

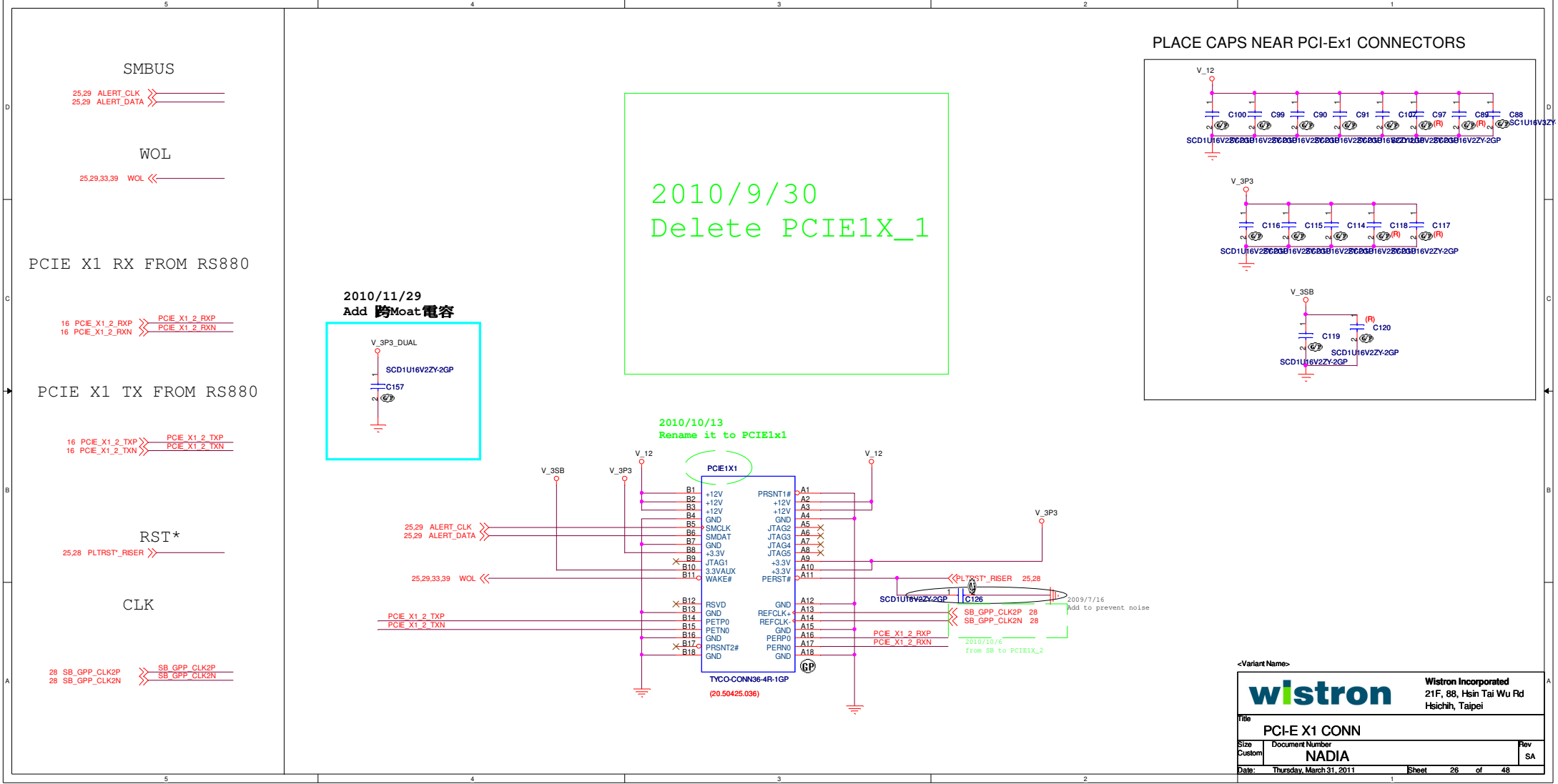


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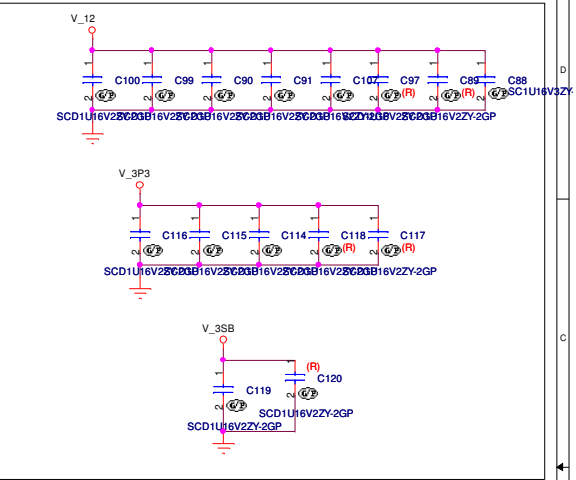
wlstron

Wistron Incorporated
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Hsichih, Taipei

File	PCI-E X16 CONN		
Size	Document Number	Rev	
Custom	NADIA	SA	
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PLACE CAPS NEAR PCI-Ex1 CONNECTORS



<Variant Name>		<div>wistron</div> <div>Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei</div>	
Title			
PCI-E X1 CONN			
Size Custom	Document Number NADIA	Rev SA	
Date:	Thursday, March 31, 2011	Sheet	26 of 48

2010/09/29

Delete PCI1 SLOT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
PCI CONN

Size Custom Document Number
NADIA

Rev
SA

Date: Thursday, March 31, 2011

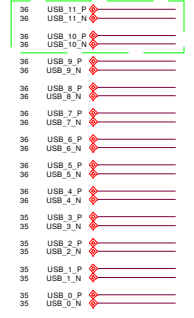
Sheet 27 of 48

35 USB_13_P

35 USB_13_N

35 USB_12_P

35 USB_12_N



```

38  AZ_BCLK    <<-----
38  AZ_SDOUT   <<-----
38  ACZ_SDIN1  <<-----
38  AZ_SYNC    <<-----
38,40 AZ_RST_N <<-----
32  AZ_SDATA_OUT <<-----

```



35 USB_OC_12_13>>
36 USB_OC_10_11>>
36 USB_OC_6_7>>
36 USB_OC_4_5>>
35 USB_OC_2_3>>
35 USB_OC_0_1>>
36 USB_OC_8_9>>

```

10,41 CPU_SIC
10,41 CPU_SID
32 SB_GPIO199
32 SB_GPIO200
41,42 USB_CTLN
USB_CTLN

```

```

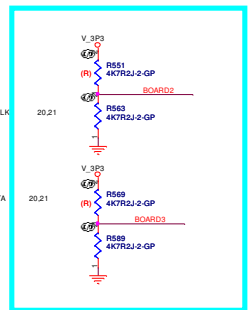
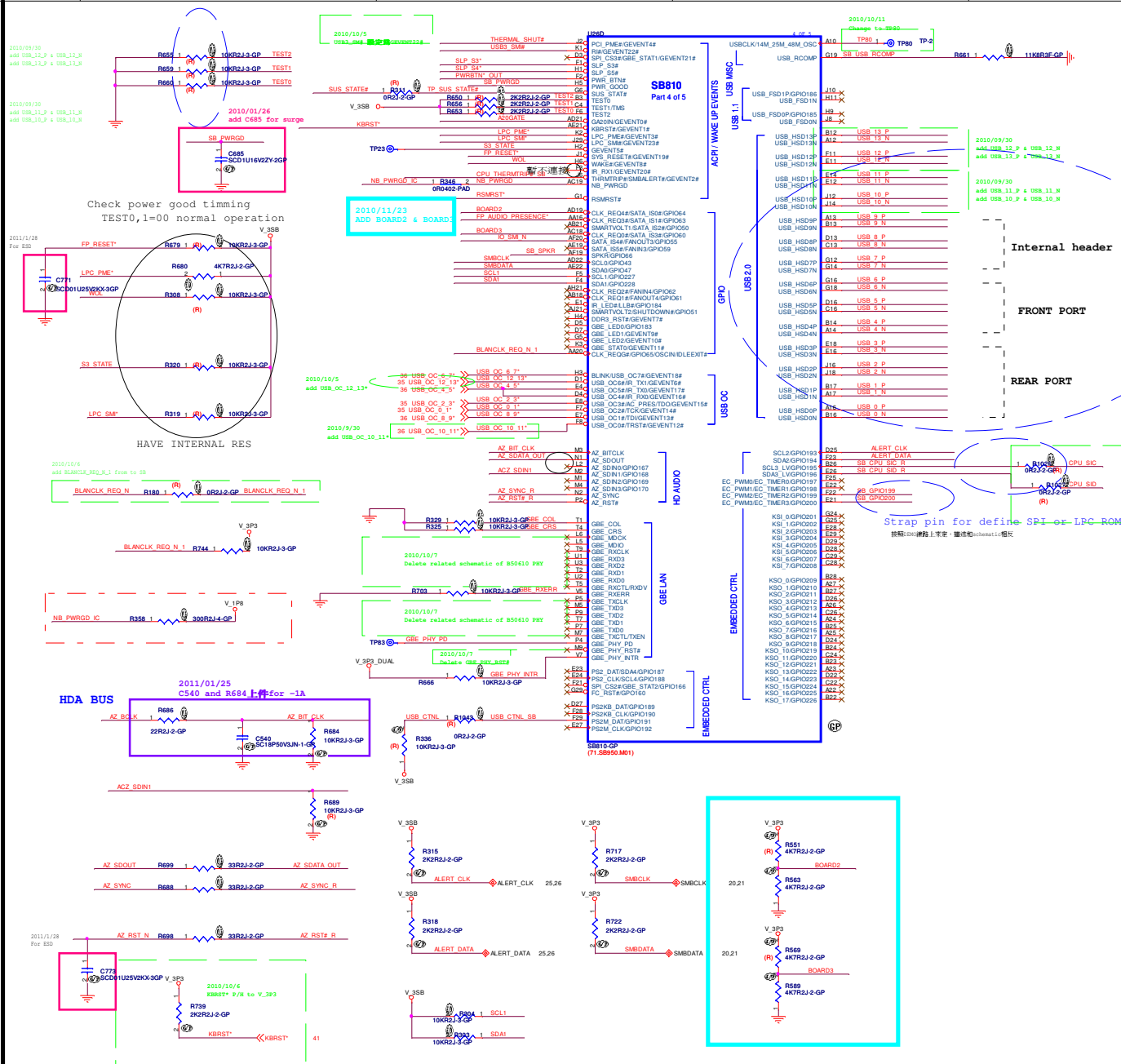
41,42,43,46 SLP_S3*
41,45 SLP_S4*
41 FWBSTN* OUT
(41,46,47 SB_PWRG*
41 AC2OATE
41 KBRST*
41 LPC_PME*

41 THERMAL_SHUTD*

33 USB3_SM#
25,26,33,39 WOL
CPU_THERMTRIP# SB
5,17 NB_PWRGD_IC
41 RSMRST*
42 FP_RESET* FP_RESET*
17 SUS_STATE# SUS_STATE#

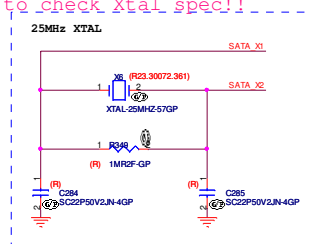
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ANCLK_REQ_N >> BLANCLK_REQ_N



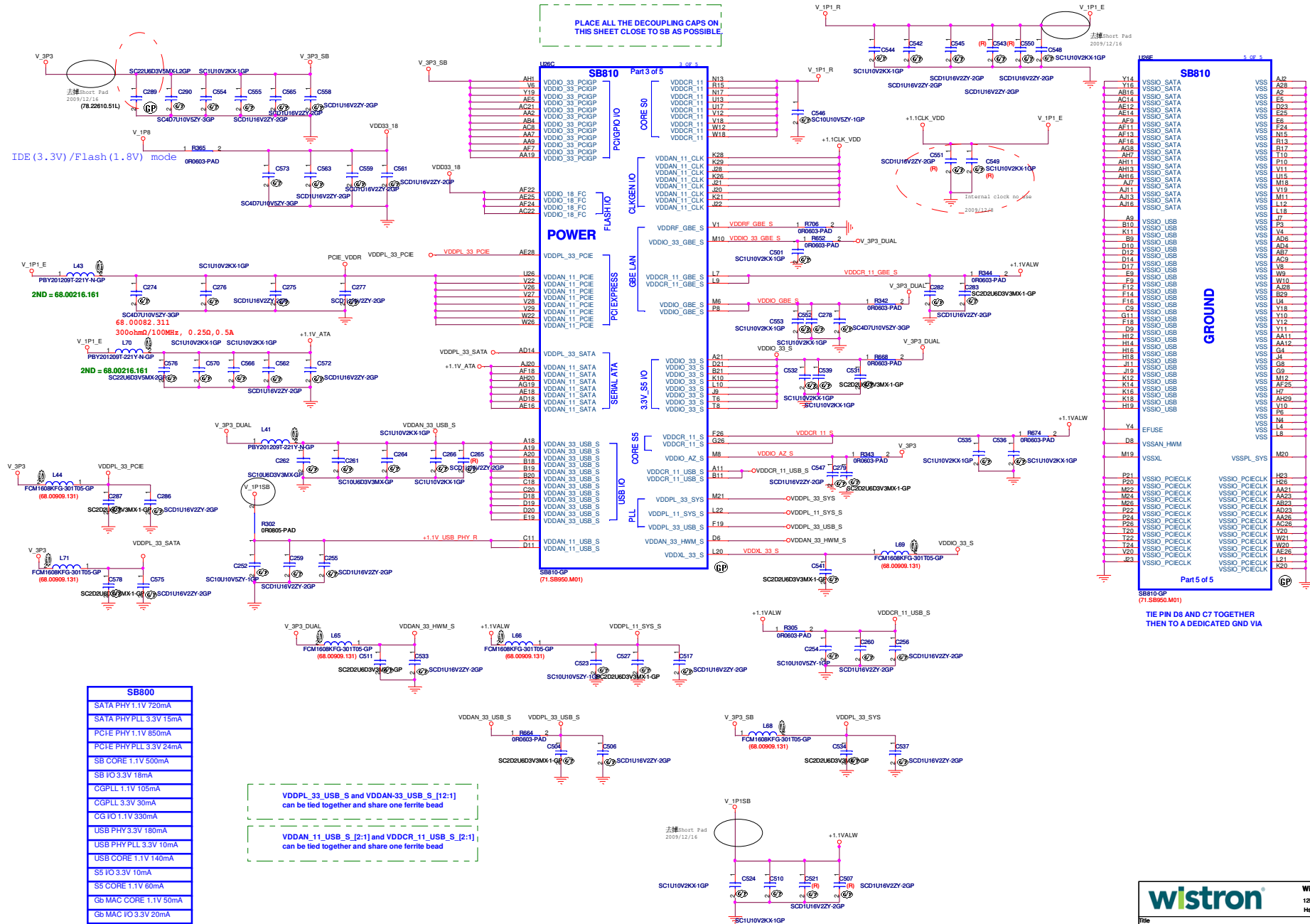


PLACE SATA_CAL
RES VERY CLOSE
TO BALLS OF U600





PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE

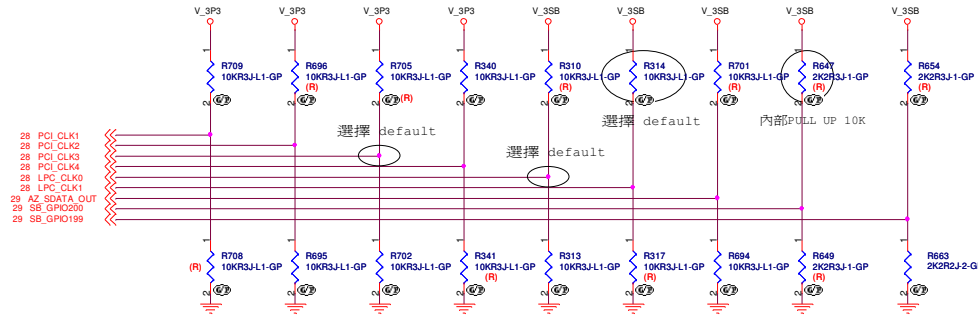


SB8800
SATA PHY 1.1V 720mA
SATA PHY PLL 3.3V 15mA
PCI-E PHY 1.1V 850mA
PCI-E PHY PLL 3.3V 24mA
SB CORE 1.1V 500mA
SB IO 3.3V 18mA
CG PLL 1.1V 105mA
CG PLL 3.3V 30mA
CG IO 1.1V 330mA
USB PHY 3.3V 180mA
USB PHY PLL 3.3V 10mA
USB CORE 1.1V 140mA
S5 IO 3.3V 10mA
SS CORE 1.1V 60mA
Gb MAC CORE 1.1V 50mA
Gb MAC IO 3.3V 20mA

TIE PIN D8 AND C7 TOGETHER
THEN TO A DEDICATED GND VIA



NOTE: SB950 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



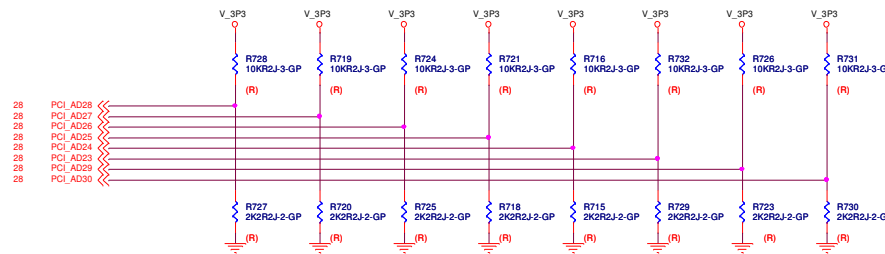
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2 DEFAULT	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE GEN1	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H = LPC ROM L, L = FWH ROM	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB950 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

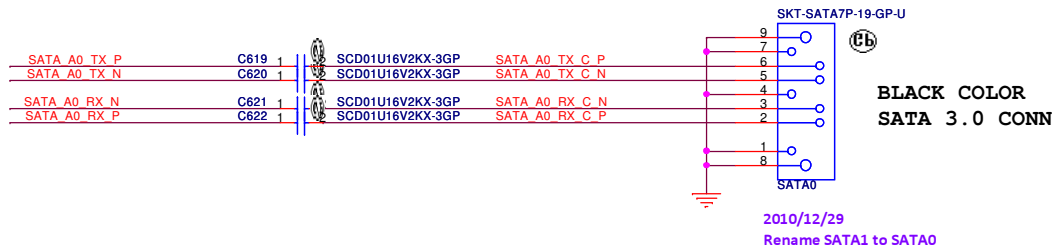


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

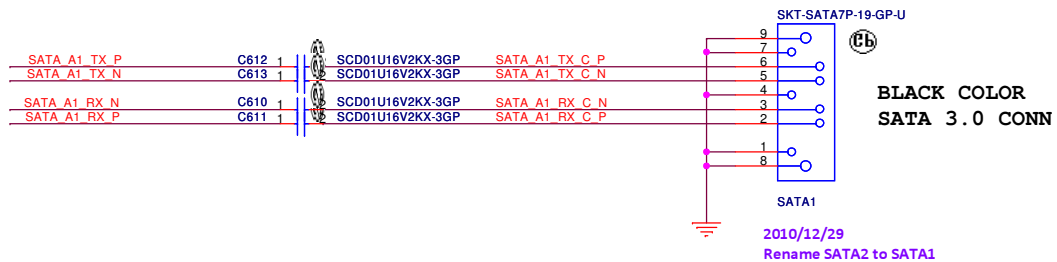
<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File STRAPS			
Size	Document Number	Rev	
Custom	NADIA	SA	
Date:	Thursday, March 31, 2011	Sheet	32 of 48

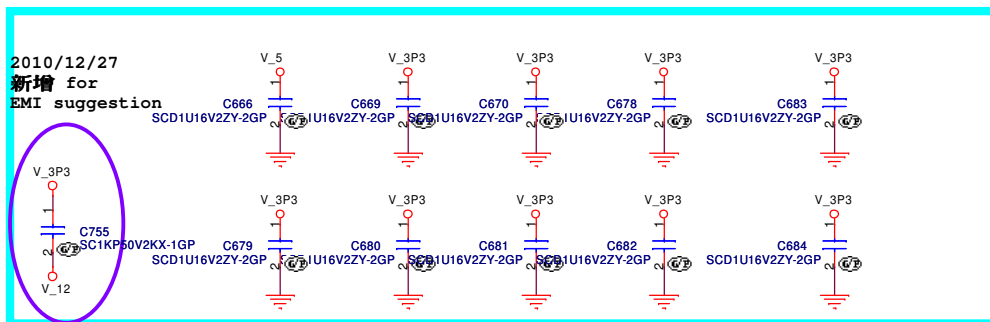
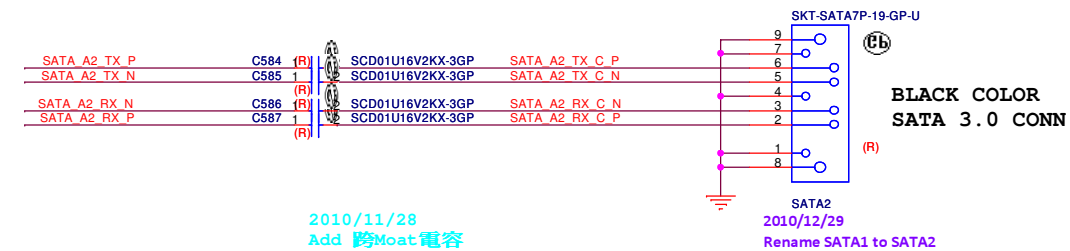
30 SATA_TXP0 >> SATA_A0_TX_P
30 SATA_TXN0 >> SATA_A0_TX_N
30 SATA_RXN0 >> SATA_A0_RX_N
30 SATA_RXP0 >> SATA_A0_RX_P




30 SATA_TXP1 >> SATA_A1_TX_P
30 SATA_TXN1 >> SATA_A1_TX_N
30 SATA_RXN1 >> SATA_A1_RX_N
30 SATA_RXP1 >> SATA_A1_RX_P



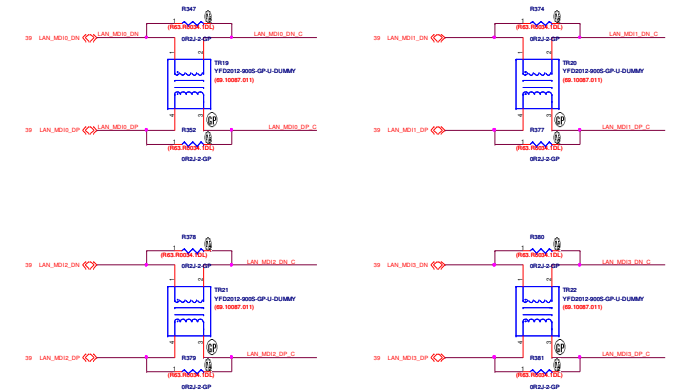
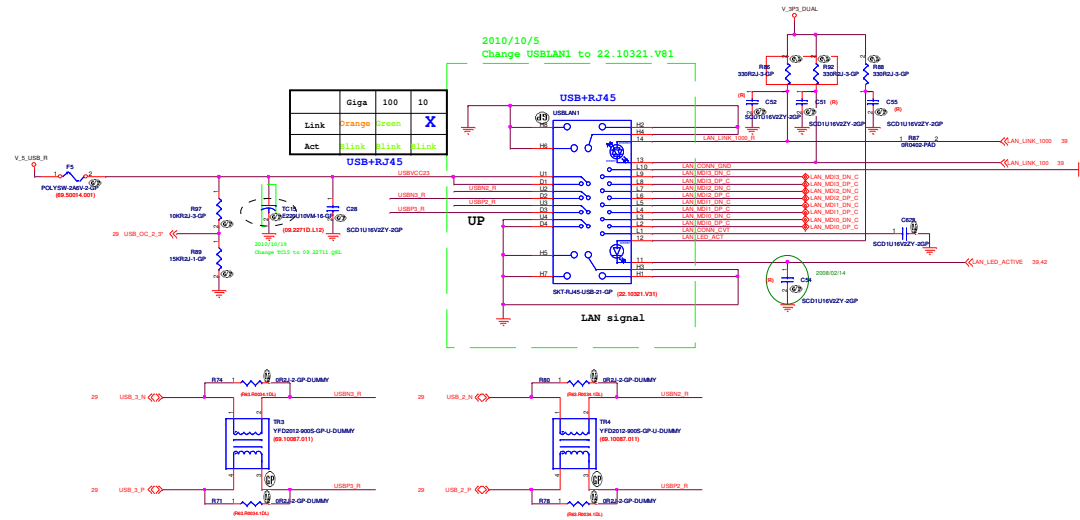
30 SATA_TXP2 >> SATA_A2_TX_P
30 SATA_TXN2 >> SATA_A2_TX_N
30 SATA_RXN2 >> SATA_A2_RX_N
30 SATA_RXP2 >> SATA_A2_RX_P



<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title SATA CONN			
Size B	Document Number NADIA		Rev SA
Date:	Thursdav, March 31, 2011	Sheet	34 of 48

Pinout diagram for the LAN connector. The connector has 10 pins. The first three pins are labeled LAN_LINK_100, LAN_LINK_1000, and LAN_LED_ACTIVE. The remaining seven pins are labeled LAN_MDIO_DIN, LAN_MDIO_DOUT, LAN_MDIO_DP, LAN_MDIO_DN, LAN_MDIO_DP, LAN_MDIO_DN, and LAN_MDIO_DP. The connector is connected to a 10-pin header with pins labeled 3_P, 3_N, 2_P, 2_N, and 3'.



20 USB_5_N

20 USB_5_P

20 USB_1_N

20 USB_1_P

2010/10/5

New add

20 USB_12_1*

20 USB_12_1*

20 USB_12_1*

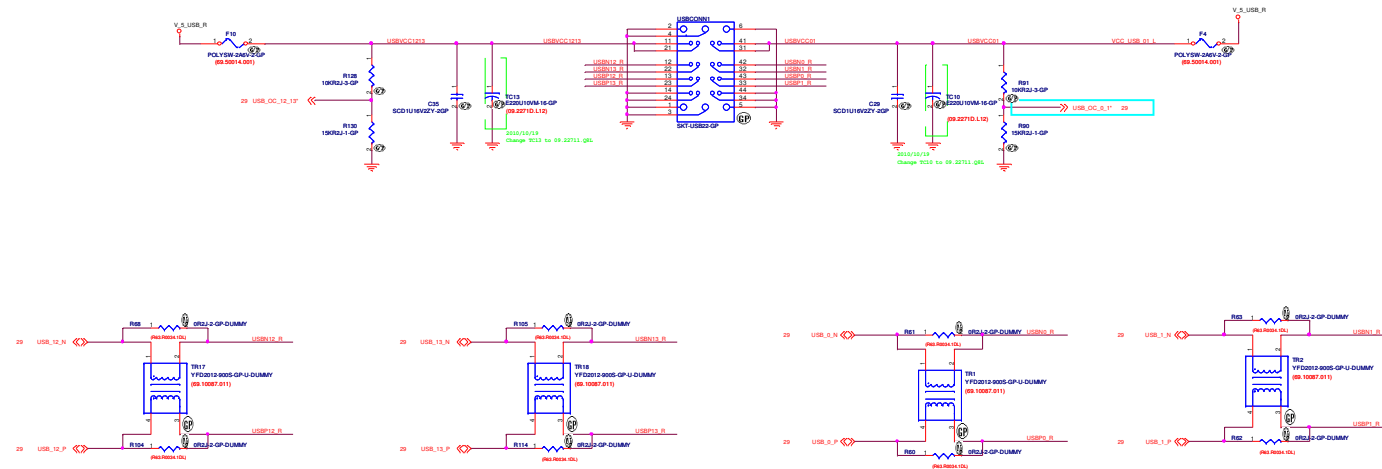
20 USB_12_1*

2010/10/5

add USB_OC_12_13*

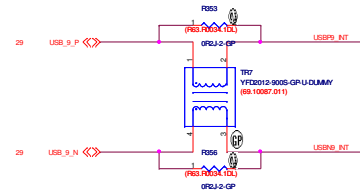
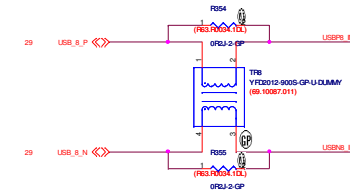
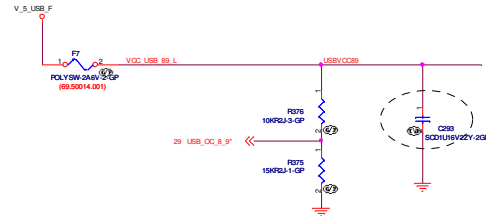
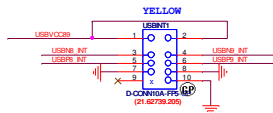
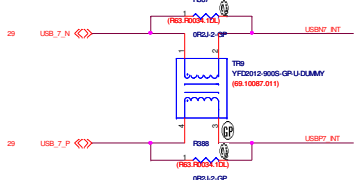
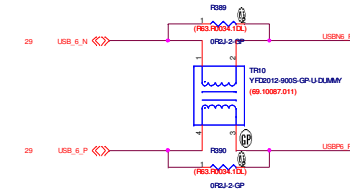
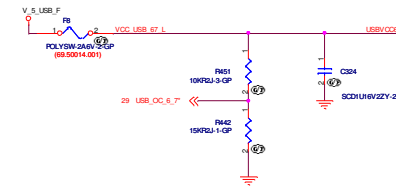
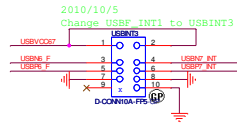
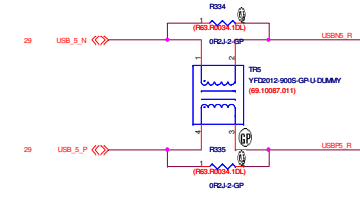
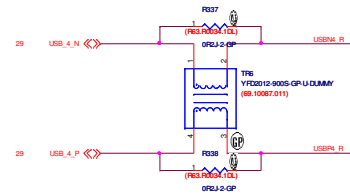
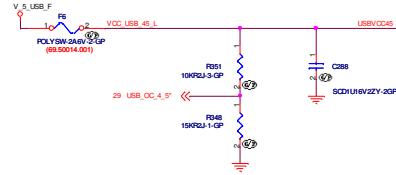
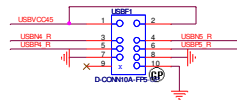
20 USB_OC_12_13*

20 USB_OC_12_13*

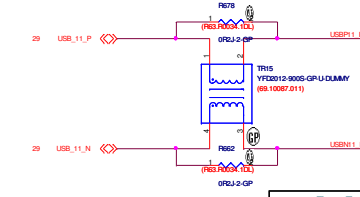
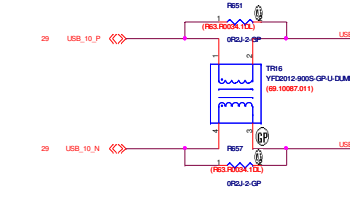
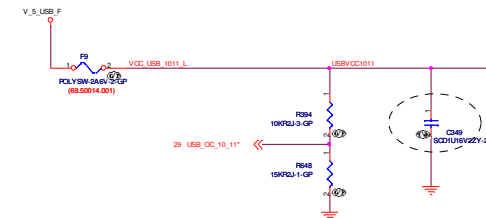
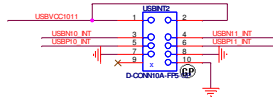


FRONT USB

29 USB_A_N <>
 29 USB_A_P <>
 29 USB_S_N <>
 29 USB_S_P <>
 29 USB_6_N <>
 29 USB_6_P <>
 29 USB_7_N <>
 29 USB_7_P <>
 29 USB_8_N <>
 29 USB_8_P <>
 29 USB_9_N <>
 29 USB_9_P <>
 29 USB_10_N <>
 29 USB_10_P <>
 29 USB_11_P <>
 29 USB_11_N <>
 29 USB_OC_4_5 <>
 29 USB_OC_6_7 <>
 2010/09/30
 add USB_OC_10_11 <>
 29 USB_OC_8_9 <>

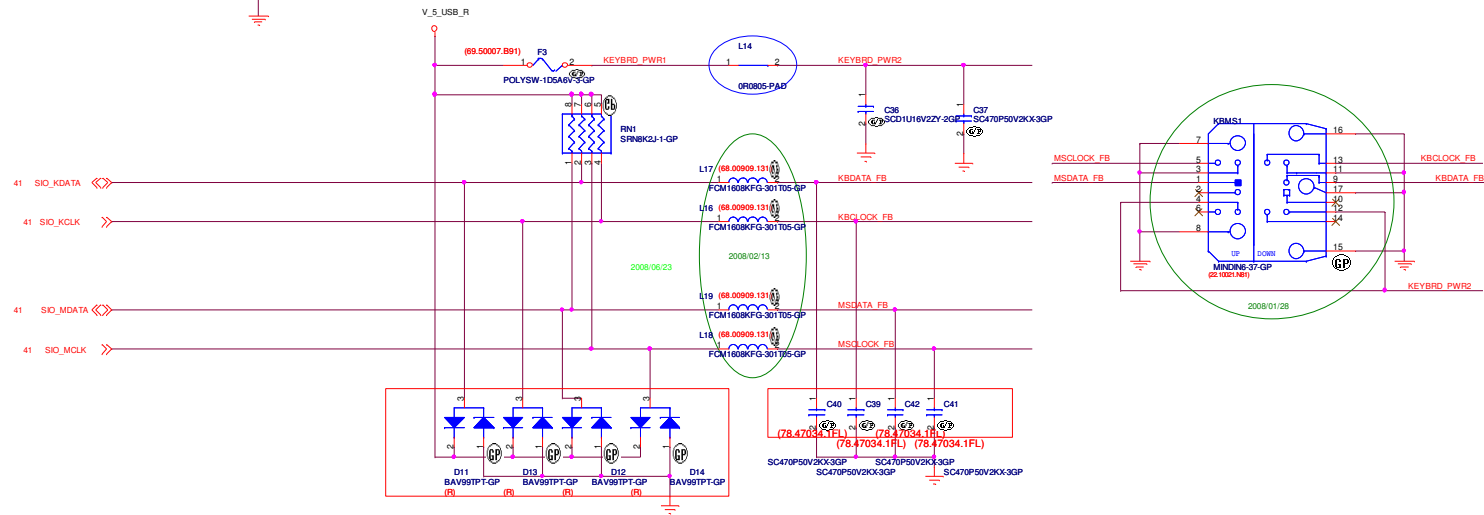


2010/09/30
 New add USBIN2 related schematic

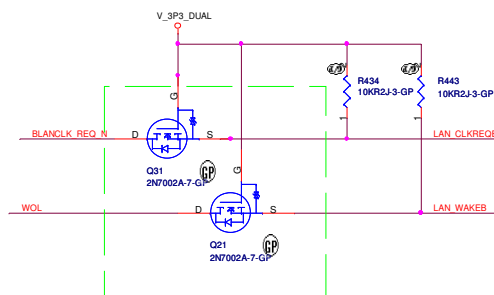
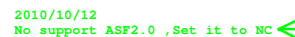
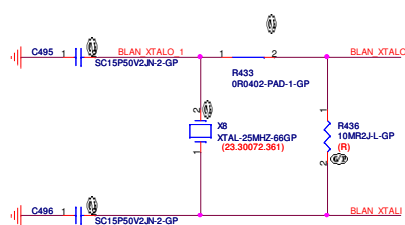
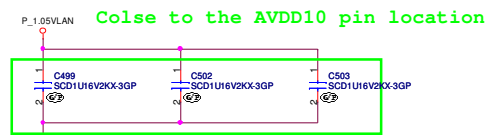
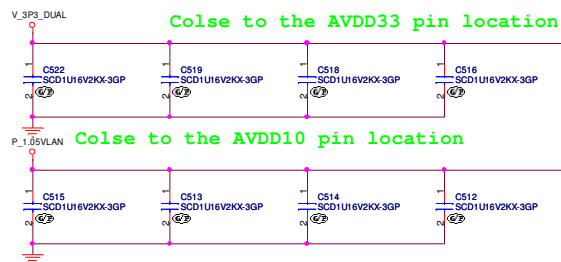


41 SIO_KCLK >>_____

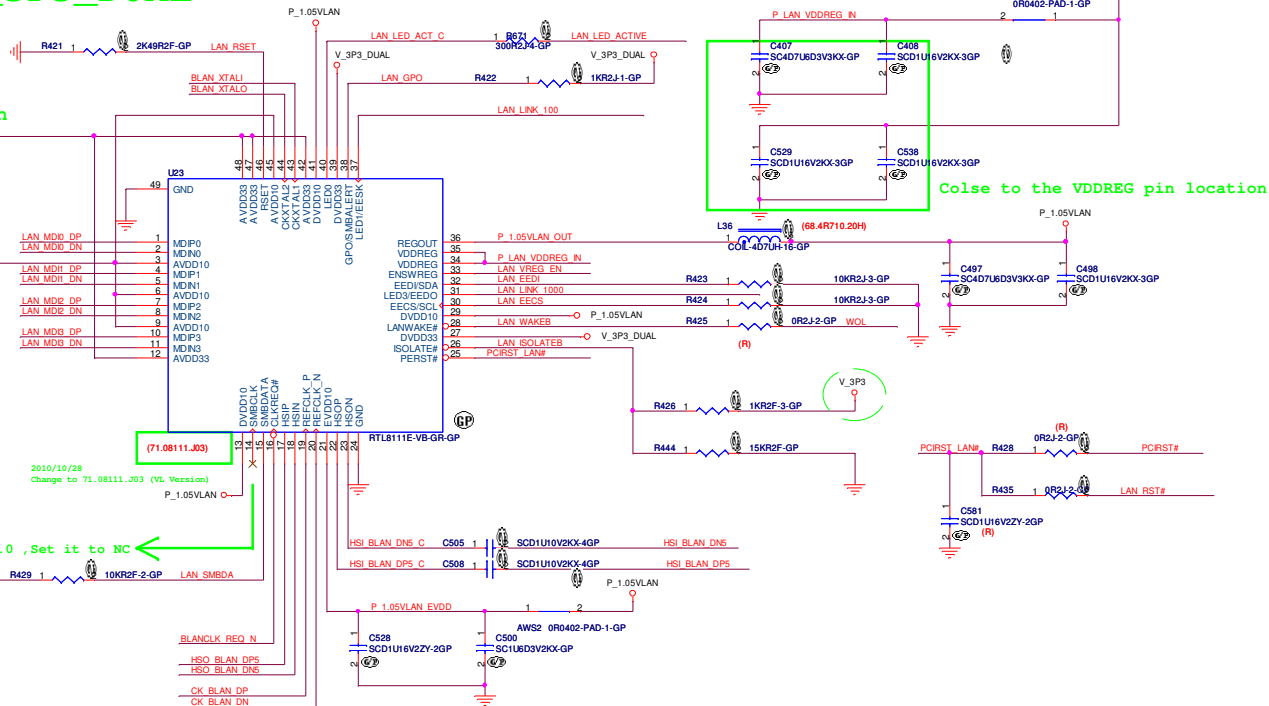
41 SID_MCLK >>



LAN POWER CHANGE TO V_3P3_DUAL



2010/10/9
CHANGE Q31 AND Q21 TO 84.2N702.E31



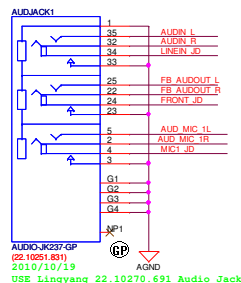
AUDIO

2010/10/5
Delete CBL14F_ID
2010/10/5
Delete CBL_OUT
2010/10/5
Delete CBL_OUT
2010/10/5
Delete SUBS_BACK_ID
2010/10/5
Delete SUBS_BACK_L
2010/10/5
Delete SUBS_BACK_R
2010/10/5
Delete SPOTF_OUT1

2010/10/5
Delete 5 port Audio Jack

Audio Jack 3 PORT CONN

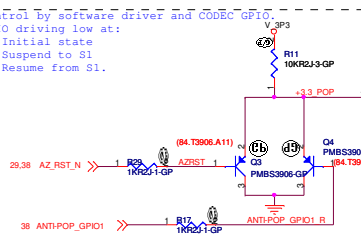
29.38 AZ_RST_N >>
38 ANTIPOP_GPIO1 >>
38 LINEIN_ID <<LINEIN_ID
38 AUD_IN_L <<AUD_IN_L
38 AUD_IN_R <<AUD_IN_R
38 FRONT_ID <<FRONT_ID
38 AUDAMPIN_L <<AUDAMPIN_L
38 AUDAMPIN_R <<AUDAMPIN_R
38 MIC1_ID <<MIC1_ID
38 MIC1_VREF0_L <<MIC1_VREF0_L
38 AUD_MIC1_L <<AUD_MIC1_L
38 AUD_MIC1_R <<AUD_MIC1_R
38 MIC1_VREF0_R <<MIC1_VREF0_R
38 FP_OUTL_LL <<FP_OUTL_LL
38 FP_OUTL_RR <<FP_OUTL_RR
38 MIC2_LL <<MIC2_LL
38 MIC2_RR <<MIC2_RR



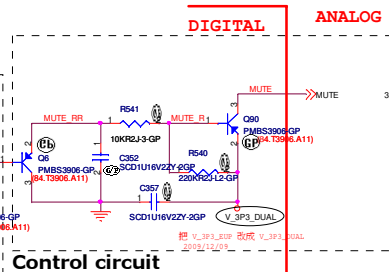
USE Lingyang 22.10270.691 Audio Jack

Rear POP Circuit

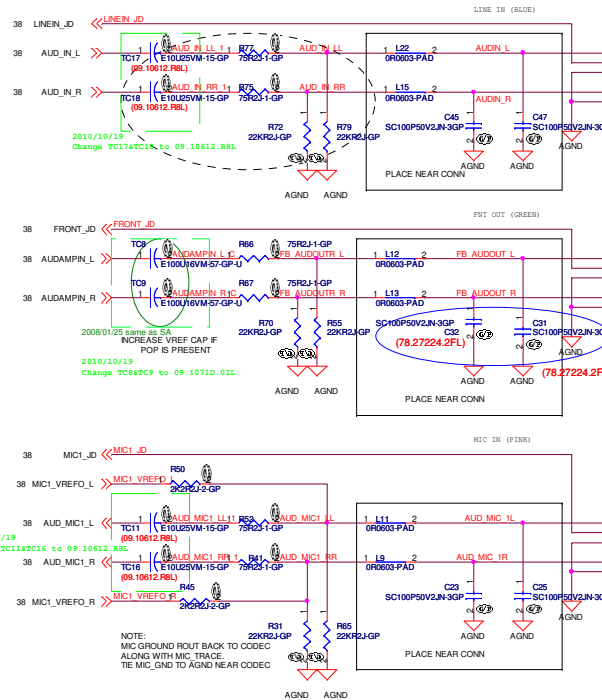
Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.



Control line



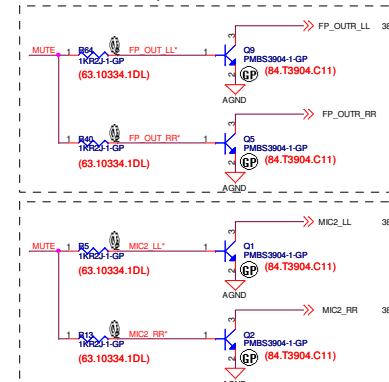
Control circuit



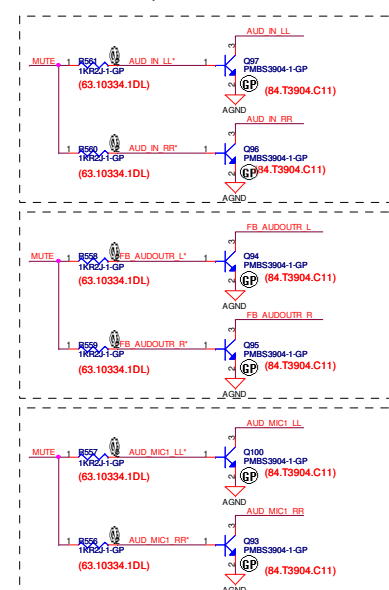
Line in
Line Out
Mic

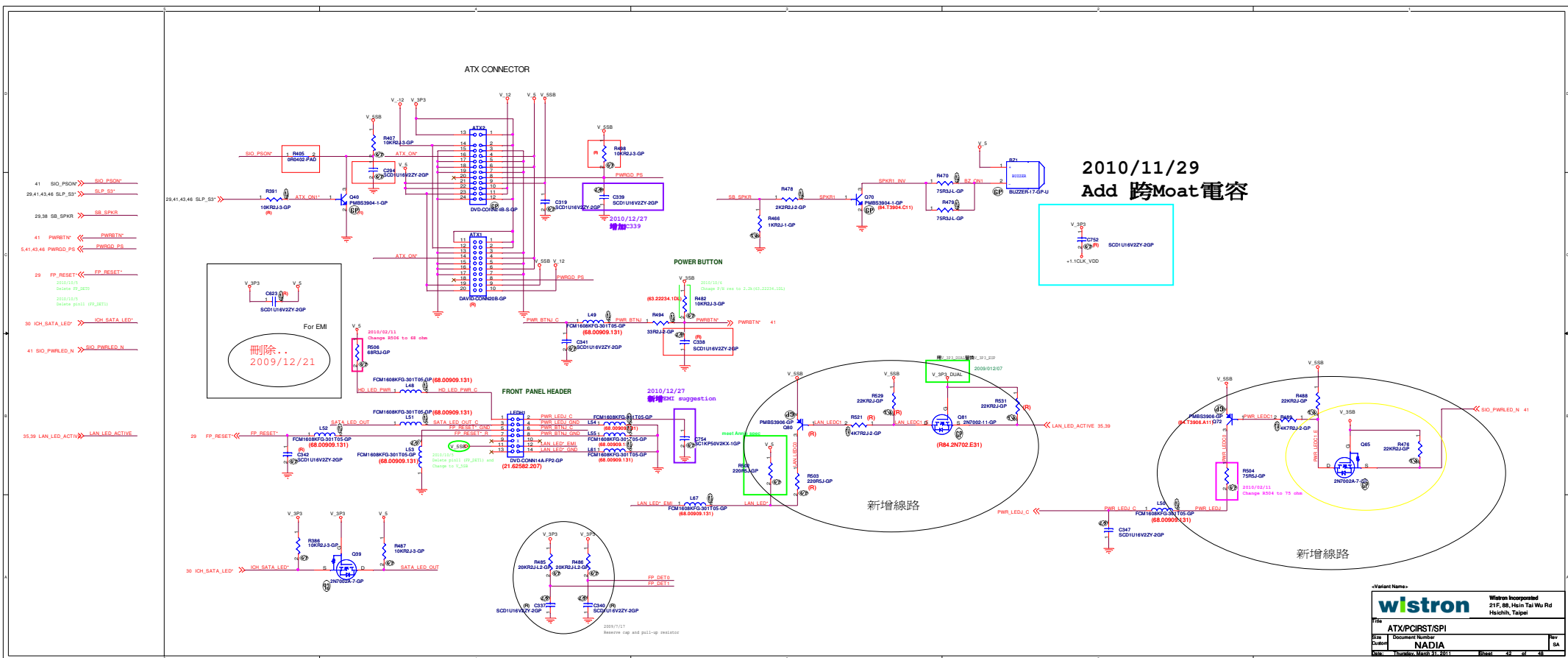
2010/10/14
Delete Mute schematic for
5 port audio jack

Front Audio Port De-Pop Circuit

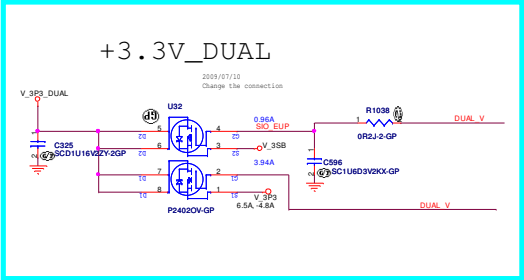
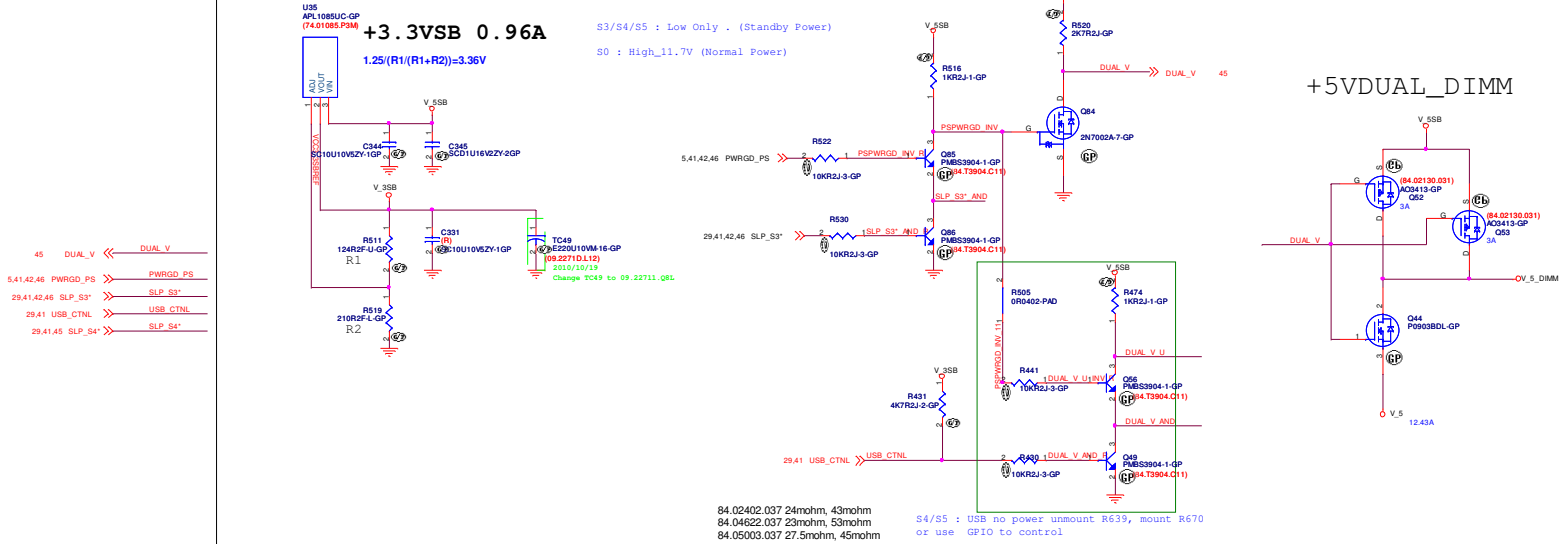


Rear Audio Port De-Pop Circuit

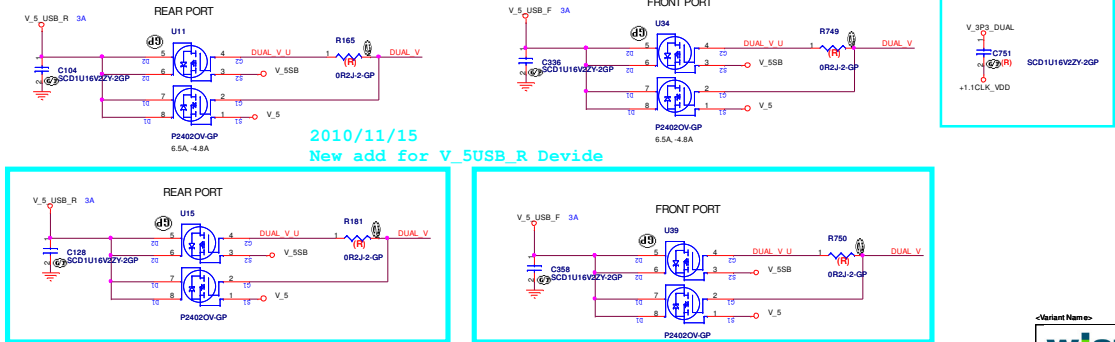




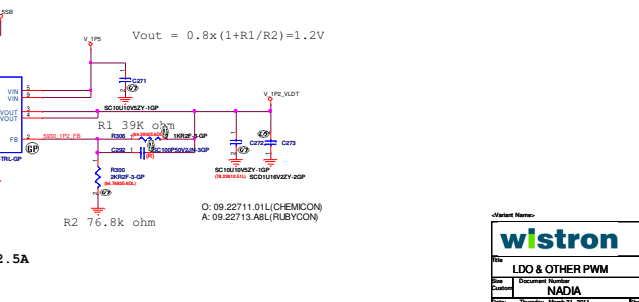
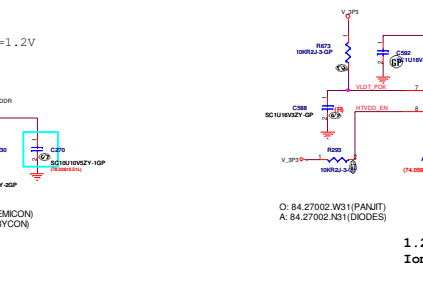
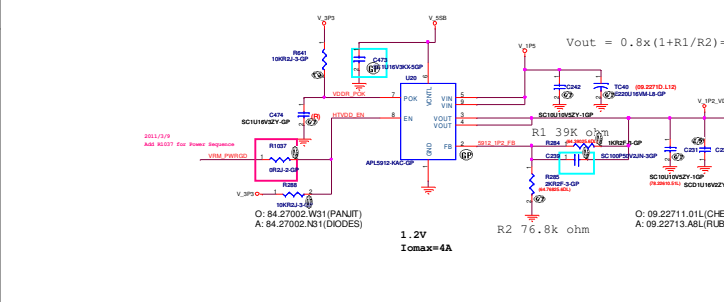
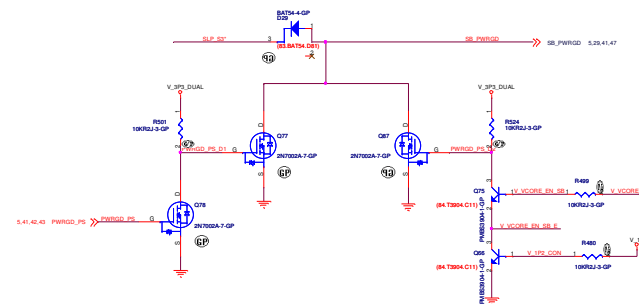
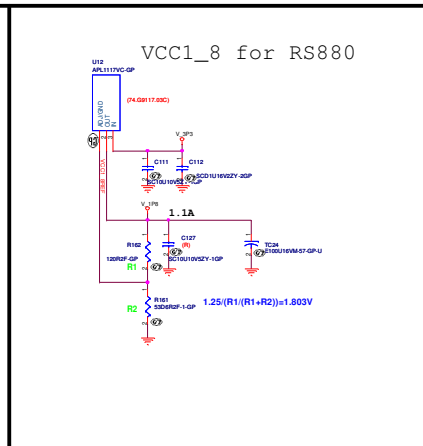
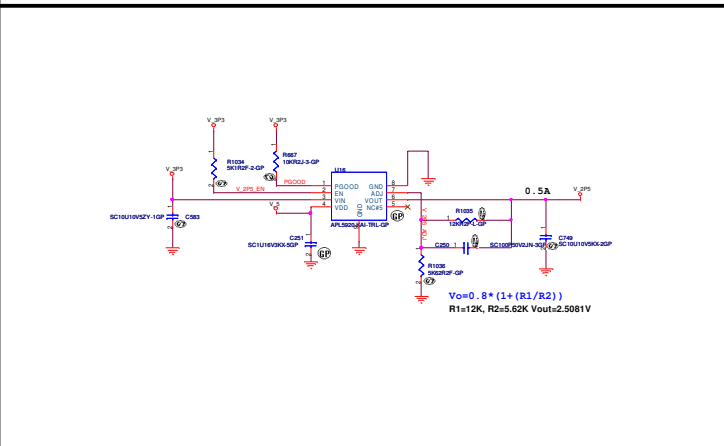
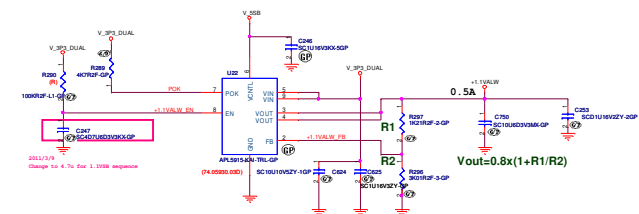
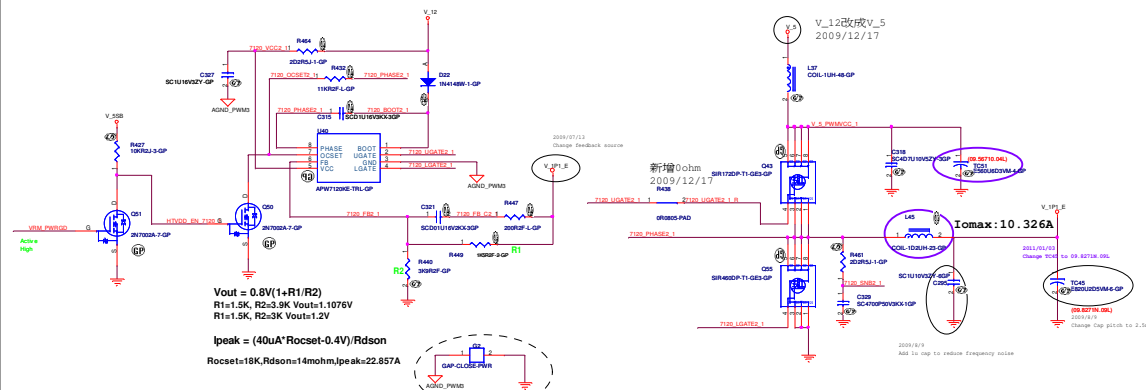
Dual Power Control



+5VDUAL_USB



-Variant Name-		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsinchu, Taipei	
File		DUAL POWER & 3.3/5V DUAL	
Size	Document Number	Rev	
Custom	NADIA	SA	
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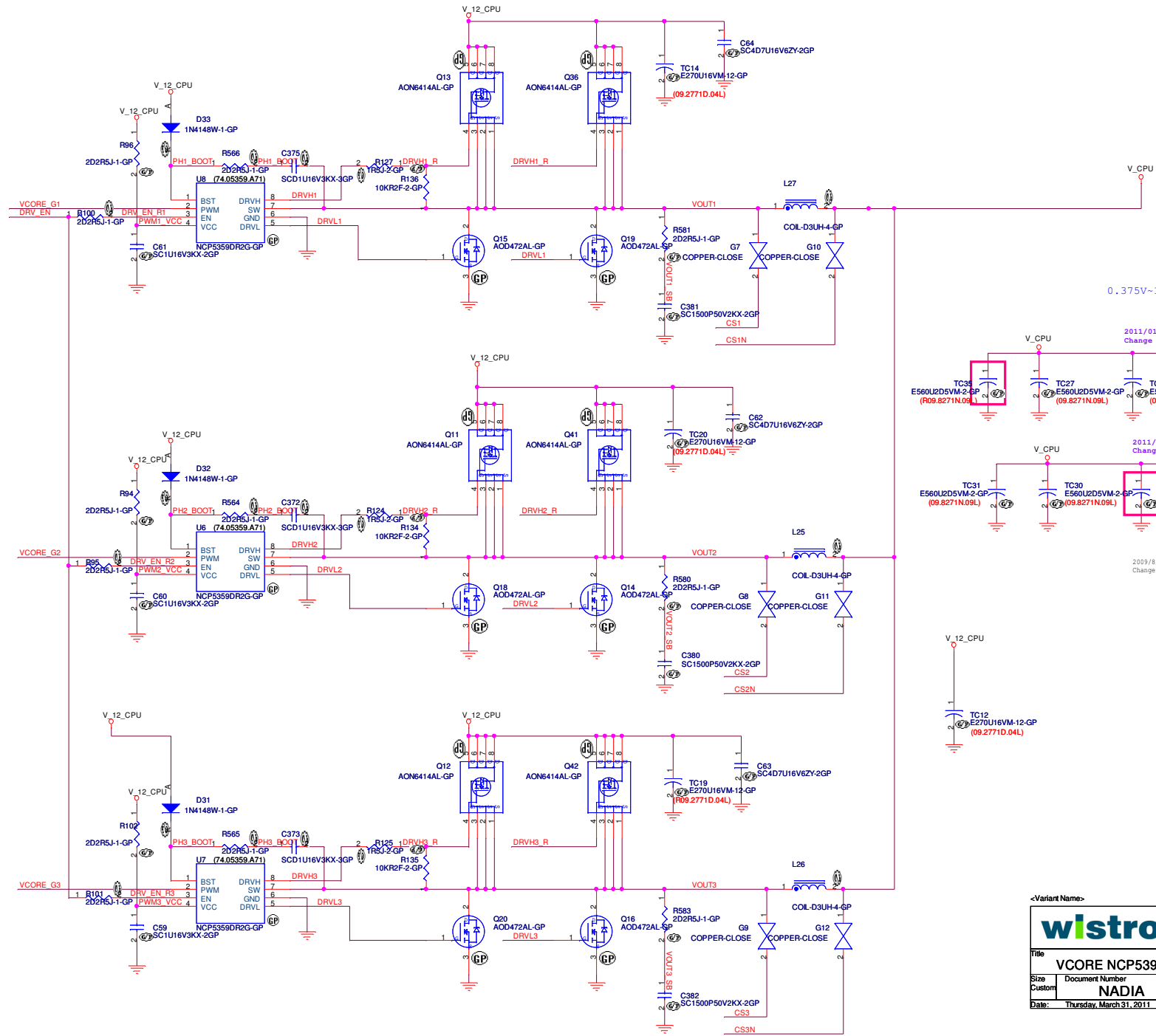


47 DRV_EN >> DRV_EN
47 VCORE_G1 >> VCORE_G1

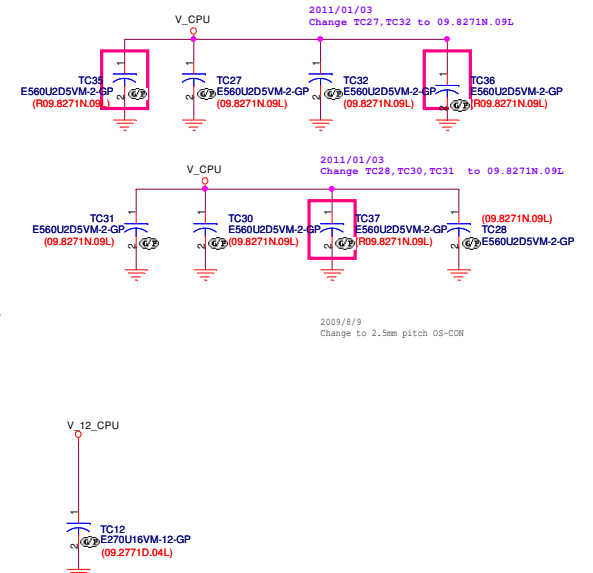
47 CS1 >> CS1
47 CS1N >> CS1N

47 VCORE_G2 >> VCORE_G2
47 CS2 >> CS2
47 CS2N >> CS2N

47 VCORE_G3 >> VCORE_G3
47 CS3 >> CS3
47 CS3N >> CS3N



0.375V~1.55V/95W



2009/8/9
Change to 2.5mm pitch 05-C0N

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
VCORE NCP5393 (2)

Size
Custom
NADIA

Date: Thursday, March 31, 2011

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Rev
SA